MT6355 PMIC Datasheet

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Document Revision History

Revision	Date	Author	Description
0.1	2016-10-21	Tim Lee	Initial draft
0.2	2016-12-07	Yunghsu Chen Jocko Kuo	1. Modified Table 2.2 pin voltage range. 2. Updated Figure 5.1 package dimension.
1.0	2017-01-19	Tim Lee	1. Added register tables. 2. Spec table re-aligned to FT results. 3. Top marking for different ordering.
1.1	2017-02-09	Tim Lee	1. Table 2-6, min. spec of short current change. 2. Added VBIF28 description in page 45. 3. Clearer Figure 5-1. 4. Modified I/O pads rating in Table2-2. 5. Modified the timing from VA10 to VIO18 in Figure 3-2 and Figure 3-3. 6. Set maximum spec of MODEM short current at Imax*3 7. Modified marking and ordering information.

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.7 ~ 5.0V
- 9 buck converters and 38 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- 26M DCXO oscillator for system timing, 1.8V and 1V clock buffer output
- SPI interface
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 226-pin FOCSP package

1.2 Applications

MT6355 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6355 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 9 buck converters and 38 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

Sophisticated controls are available for power-up, and the RTC alarm. MT6355 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6355 adopts SPI interface and two SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6355 is available in a 226-pin FOCSP package. The operating temperature ranges from -30 to +85°C.

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1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6355W/A		-30 ~ +85°C	FOCSP 226L
MT6355AEW/A		-30 ~ +85°C	FOCSP 226L
MT6355VNW/A		-30 ~ +85°C	FOCSP 226L

1.5 Top Marking Definition

MEDIATEK
MT6355W
YYWW-A$$H
$$$$$$$

MEDIATEK
MT6355AEW
YYWW-A$$H
$$$$$$$

MEDIATEK
MT6355VNW
YYWW-A$$H
$$$$$$$

YYWW : Date Code
$: Random Code

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1.6 Pin Assignments and Descriptions

224	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	GND_VS1	VS1	VSYS_VS1	VSYS_VPA1	VPA1	VSYS_VMODEM	VMODEM	GND_VMODEM	GND_VPROC1	VPROC1	VSYS_VPROC1	VSYS_VPROC2	VPROC2	GND_VPROC2	GND_VCORE	GND_VCORE	NC	A
B	GND_VS1	VS1	VSYS_VS1				VMODEM	GND_VMODEM	GND_VPROC1	VPROC1	VSYS_VPROC1	VSYS_VPROC2	VPROC2	GND_VPROC2		VCORE	VCORE	B
C	GND_VS1					GND_VPA1										VSYS_VCORE	VSYS_VCORE	C
D	GND_BUCK_CTRL1	DVDD12_IO	VS1_FB	VSYS_BUCK_CTRL1	VPA1_FB	VMODEM_FB	GND_VMODEM_FB		GND_VPROC1_FB	VPROC1_FB	GND_VPROC2_FB	VPROC2_FB	GND_VCORE_FB	VCORE_FB		VSYS_VGPU	VSYS_VGPU	D
E		VS1_SLDO2	VIO18	VCAMIO	VRF18_1	VMIPI	DVDD18_IO	FSOURCE	SPI_CSN		SPI_CLK			VSYS_BUCK_PW		VGPU	VGPU	E
F	RTC32K_1V8_1		VUFS18_S	VS1_SLDO3		VSYS_LDOS4		RTC32K_1V8_0	SPI_MISO	SPI_MOSI	AUD_DAT_MISO	SCP_VREQ_VAO	GND_VGPU_FB	VGPU_FB		GND_VGPU	GND_VGPU	F
G		VS1_SLDO1	VUFS18	VCN18	VRF18_2	VXO18		DVSS18_IO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	VOW_CLK_MISO			VSYS_VDRAM1	VDRAM1	G
H		AU_V18N		AU_HPR	AU_LOLN			DVSS18_DIG	GND_LDO	GND_LDO	GND_LDO	AUD_DAT_MOSI	GND_VDRAM_FB	VDRAM_FB1		GND_VDRAM1	VSYS_VDRAM2	H
J	FLYN	AVSS18_AUD	AU_HPL	AUDREFN	AU_LOLP	AU_HSP	AUD_TESTIN	GND_LDO	GND_LDO	GND_LDO	GND_LDO	AUD_CLK		VDRAM_FB2		VDRAM2	GND_VDRAM2	J
K	FLYP	AVDD18_AUD				AU_HSN	HOMEKEY	WDTRSTB_IN	GND_LDO	GND_LDO	GND_LDO	RESETB	PWRKEY	VS2_FB		VSYS_VS2	VSYS_VS2	K
L		AVSS30_AUD	ACCDET	AU_VIN0_P	AU_VIN0_N		AU_MICBIAS0	GND_LDO	GND_LDO	GND_LDO	GND_LDO		UVLO_VTH	EXT_PMIC_PG		VS2	VS2	L
M	AU_VIN1_N	AU_VIN1_P	AU_VIN2_N		AVDD30_AUD	AU_MICBIAS1	VCDT	CHRLDO	DVSS18_IO_2	BATADC	BATON	BATID	GND_VREF	VSRAM_CORE	VSRAM_GPU	EXT_PMIC_EN	GND_VS2	M
N	AVDD18_CODEC	AU_VIN2_P			AU_MICBIAS2	PMU_TEST_MODE	DVDD18_DIG		VSYSSNS	VSIM2	CS_P	CS_N	VREF	VSYS_DRIVER	VS2_SLDO2			N
P	SRCLKEN_IN0		XO_AUD	XO_SOC	SRCLKEN_IN1	RTC32K_2V8		VA18	VCN28	VUSB33		VMC	VLDO28	VSRAM_MD	VSRAM_PROC	VA10		P
R	XO_WCN	XO_CEL	XO_EXT	XO_NFC		AVDD28_VRTC	VGP2	VXO22		VSYS_LDOS1	VSYS_LDOS2	VCN33	VSYS_LDOS3	VRF12	VS2_SLDO1	VA12	VA12	R
T	AVSS22_XOBUF	AVSS22_XO	AVSS22_XOBUF	VXO18_LV	AVDD18_AUXADC		AVSS18_AUXADC	VTCXO24	VCAMA1	VFE28	VMCH	VEMC	VIO28	VCAMD2	VS2_SLDO3	VCAMD1	VCAMD1_S	T
U	NC	XTAL1	XTAL2	AVSS_XO_ISO	AUXADC_VIN	XIN	XOUT	VCAMA2		VBIF28	VGP	VSIM1			VCAMD2_S	VCAMD1	NC	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 1-1. MT6355 FOCSP 226 (6.8x6.8mm) pin assignment (top view)

Table 1-1. MT6355 pin descriptions

Ball	Symbol	I/O	Description
A1	GND_VS1	GND	VS1 ground
A2	VS1	O	SW node of VS1

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Ball	Symbol	I/O	Description
A3	VSYS_VS1	PWR	Power supply of VS1
A4	VSYS_VPA1	PWR	Power supply of VPA
A5	VPA1	O	SW node of VPA
A6	VSYS_VMODEM	PWR	Power supply of VMODEM
A7	VMODEM	O	SW node of VMODEM
A8	GND_VMODEM	GND	VMODEM ground
A9	GND_VPROC1	GND	VPROC1 ground
A10	VPROC1	O	SW node of VPROC1
A11	VSYS_VPROC1	PWR	Power supply of VPROC1
A12	VSYS_VPROC2	PWR	Power supply of VPROC2
A13	VPROC2	O	SW node of VPROC2
A14	GND_VPROC2	GND	VPROC2 ground
A15	GND_VCORE	GND	VCORE ground
A16	GND_VCORE	GND	VCORE ground
B1	GND_VS1	GND	VS1 ground
B2	VS1	O	SW node of VS1
B3	VSYS_VS1	PWR	Power supply of VS1
B7	VMODEM	O	SW node of VMODEM
B8	GND_VMODEM	GND	VMODEM ground
B9	GND_VPROC1	GND	VPROC1 ground
B10	VPROC1	O	SW node of VPROC1
B11	VSYS_VPROC1	PWR	Power supply of VPROC1
B12	VSYS_VPROC2	PWR	Power supply of VPROC2
B13	VPROC2	O	SW node of VPROC2
B14	GND_VPROC2	GND	VPROC2 ground
B16	VCORE	O	SW node of VCORE
B17	VCORE	O	SW node of VCORE
C1	GND_VS1	GND	VS1 ground
C6	GND_VPA1	GND	VPA ground
C16	VSYS_VCORE	PWR	Power supply of VCORE
C17	VSYS_VCORE	PWR	Power supply of VCORE
D1	GND_BUCK_CTRL1	GND	GND of BUCK CTRL
D2	DVDD12_IO	PWR	DVDD12 IO power
D3	VS1_FB	I	BUCK VS1 feedback pin
D4	VSYS_BUCK_CTRL1	PWR	Power supply of buck controller
D5	VPA1_FB	I	BUCK VPA feedback pin
D6	VMODEM_FB	I	BUCK VMODEM feedback pin
D7	GND_VMODEM_FB	I	Remote sense on ground of VMODEM
D9	GND_VPROC1_FB	GND	BUCK VPROC1 GND feedback pin
D10	VPROC1_FB	I	BUCK VPROC1 feedback pin
D11	GND_VPROC2_FB	GND	BUCK VPROC2 GND feedback pin
D12	VPROC2_FB	I	BUCK VS1 feedback pin
D13	GND_VCORE_FB	I	Remote sense on ground of VCORE
D14	VCORE_FB	I	BUCK VCORE feedback pin
D16	VSYS_VGPU	PWR	Power supply of VGPU
D17	VSYS_VGPU	PWR	Power supply of VGPU
E2	VS1_SLDO2	PWR	2.1V power supply of SLDO2

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Ball	Symbol	I/O	Description
E3	VIO18	O	VIO18 output voltage
E4	VCAMIO	O	VCAMIO output voltage
E5	VRF18_1	O	VRF18_1 output voltage
E6	VMIPI	O	VMIPI output voltage
E7	DVDD18_IO	PWR	Digital IO power
E8	FSOURCE	PWR	EFUSE power source
E9	SPI_CSN	IO	SPI control interface
E11	SPI_CLK	I	SPI control interface
E14	VSYS_BUCK_PW	PWR	Power supply of BUCK power mos N-well
E16	VGPU	O	SW node of VGPU
E17	VGPU	O	SW node of VGPU
F1	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
F3	VUFS18_S	O	VUFS18 output sense
F4	VS1_SLDO3	PWR	Power supply of SLDO3
F6	VSYS_LDOS4	PWR	Power supply input of SLDO20
F8	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
F9	SPI_MISO	IO	SPI control interface
F10	SPI_MOSI	IO	SPI control interface
F11	AUD_DAT_MISO	IO	Audio control interface
F12	SCP_VREQ_VAO	IO	SCP_VREQ_VAO
F13	GND_VGPU_FB	I	Remote sense on ground of VGPU
F14	VGPU_FB	I	BUCK VGPU feedback pin
F16	GND_VGPU	GND	VGPU ground
F17	GND_VGPU	GND	VGPU ground
G2	VS1_SLDO1	PWR	2.1V power supply of SLDO1
G3	VUFS18	O	VUFS18 output voltage
G4	VCN18	O	VCN18 output voltage
G5	VRF18_2	O	VRF18_2 output voltage
G6	VXO18	O	VXO18 output voltage
G8	DVSS18_IO	GND	Digital IO GND
G9	GND_LDO	GND	LDO ground
G10	GND_LDO	GND	LDO ground
G11	GND_LDO	GND	LDO ground
G12	GND_LDO	GND	LDO ground
G13	VOW_CLK_MISO	IO	VOW_CLK_MISO
G16	VSYS_VDRAM1	PWR	Power supply of VDRAM1
G17	VDRAM1	O	SW node of VDRAM1
H2	AU_V18N	PWR	Audio -1.8V supply
H4	AU_HPR	O	Earphone right channel output
H5	AU_LOLN	O	Negative output of line-out buffer
H8	DVSS18_DIG	GND	GND of DIG DVSS18
H9	GND_LDO	GND	LDO ground
H10	GND_LDO	GND	LDO ground
H11	GND_LDO	GND	LDO ground
H12	AUD_DAT_MOSI	IO	Audio control interface
H13	GND_VDRAM_FB1	GND	BUCK VDRAM1 GND feedback pin
H14	VDRAM_FB1	I	BUCK VDRAM1 feedback pin

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Ball	Symbol	I/O	Description
H16	GND_VDRAM1	GND	GND of VDRAM1
H17	VSYS_VDRAM2	PWR	Power supply of VDRAM2
J1	FLYN	O	Flying capacitor bottom
J2	AVSS18_AUD	GND	Audio DL ground
J3	AU_HPL	O	Earphone left channel output
J4	AUDREFN	GND	Audio reference ground
J5	AU_LOLP	O	Positive output of line-out buffer
J6	AU_HSP	O	Handset positive output
J7	AUD_TESTIN	I	Audio input pin under audio test mode
J8	GND_LDO	GND	LDO ground
J9	GND_LDO	GND	LDO ground
J10	GND_LDO	GND	LDO ground
J11	GND_LDO	GND	LDO ground
J12	AUD_CLK	I	Audio control interface
J14	VDRAM_FB2	I	BUCK VDRAM2 feedback pin
J16	VDRAM2	O	SW node of VDRAM2
J17	GND_VDRAM2	GND	GND of VDRAM2
K1	FLYP	O	Flying capacitor top
K2	AVDD18_AUD	PWR	1.8V power supply of Audio
K6	AU_HSN	O	Handset negative output
K7	HOMEKEY	I	Home key
K8	WDTRSTB_IN	I	Watchdog reset from AP
K9	GND_LDO	GND	LDO ground
K10	GND_LDO	GND	LDO ground
K11	GND_LDO	GND	LDO ground
K12	RESETB	O	System reset release signal
K13	PWRKEY	I	PWRKEY button
K14	VS2_FB	I	BUCK VS2 feedback pin
K16	VSYS_VS2	PWR	Power supply of VS2
K17	VSYS_VS2	PWR	Power supply of VS2
L2	AVSS30_AUD	GND	Audio UL ground
L3	ACCDET	I	Accessory detection input 1
L4	AU_VIN0_P	I	Microphone channel 0 positive input
L5	AU_VIN0_N	I	Microphone channel 0 negative input
L7	AU_MICBIAS0	O	Microphone Bias 0
L8	GND_LDO	GND	LDO ground
L9	GND_LDO	GND	LDO ground
L10	GND_LDO	GND	LDO ground
L11	GND_LDO	GND	LDO ground
L13	UVLO_VTH	I	UVLO threshold control pin
L14	EXT_PMIC_PG	I	External PMIC PG
L16	VS2	O	SW node of VS2
L17	VS2	O	SW node of VS2
M1	AU_VIN1_N	I	Microphone channel 1 negative input
M2	AU_VIN1_P	I	Microphone channel 1 positive input
M3	AU_VIN2_N	I	Microphone channel 2 negative input
M5	AVDD30_AUD	PWR	Power supply of Audio UL

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Ball	Symbol	I/O	Description
M6	AU_MICBIAS1	O	Microphone Bias 1
M7	VCDT	I	Fractional charger input voltage for charger detection
M8	CHRLDO	O	CHRLDO output voltage
M9	DVSS18_IO_2	GND	Digital IO GND
M10	BATADC	I	Battery ADC sense
M11	BATON	I	Battery NTC pin for battery and its temperature sensing
M12	BATID	I	Battery ID
M13	GND_VREF	GND	Ground for bandgap
M14	VSRAM_CORE	O	VSRAM_CORE output voltage
M15	VSRAM_GPU	O	VSRAM_GPU output voltage
M16	EXT_PMIC_EN	IO	Ext chip MT6311/MT6313 enable pin
M17	GND_VS2	GND	VS2 ground
N1	AVDD18_CODEC	PWR	Power supply of CODEC
N2	AU_VIN2_P	I	Microphone channel 2 positive input
N5	AU_MICBIAS2	O	Microphone Bias 2
N6	PMU_TEST_MODE	I	PMU test mode signal (tied to GND in normal operation)
N7	DVDD18_DIG	O	VDIG18 output voltage
N9	VSYSSNS	PWR	VSYS supply input for internal block and UVLO detection
N10	VSIM2	O	VSIM2 output voltage
N11	CS_P	I	Fuel gauge ADC input pin
N12	CS_N	I	Fuel gauge ADC input pin
N13	VREF	O	Bandgap reference voltage
N14	VSYS_DRIVER	PWR	Power supply of ISINK driver
N15	VS2_SLDO2	PWR	1.35V power supply of SLDO2
P1	SRCLKEN_IN0	I	Source clock enable pin 0
P3	XO_AUD	O	26MHz output to Audio
P4	XO_SOC	O	26MHz output to SOC
P5	SRCLKEN_IN1	I	Source clock enable pin 1
P6	RTC32K_2V8	O	VRTC domain 32kHz clock output
P8	VA18	O	VA18 output voltage
P9	VCN28	O	VCN28 output voltage
P10	VUSB33	O	VUSB33 output voltage
P12	VMC	O	VMC output voltage
P13	VLDO28	O	VLDO28 output voltage
P14	VSRAM_MD	O	SW node of VSRAM_MD
P15	VSRAM_PROC	O	VSRAM_PROC output voltage
P16	VA10	O	VA10 output voltage
R1	XO_WCN	O	26MHz output to Conn. RF
R2	XO_CEL	O	26MHz output to Cell. RF
R3	XO_EXT	O	26MHz output to EXT
R4	XO_NFC	O	26MHz output to NFC
R6	AVDD28_VRTC	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
R7	VGP2	O	VGP2 output voltage

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Ball	Symbol	I/O	Description
R8	VXO22	O	VXO22 output voltage
R10	VSYS_LDOS1	PWR	Power supply input of LDO group 1
R11	VSYS_LDOS2	PWR	Power supply input of LDO group 2
R12	VCN33	O	VCN33 output voltage
R13	VSYS_LDOS3	PWR	Power supply input of LDO group 3
R14	VRF12	O	VRF12 output voltage
R15	VS2_SLDO1	PWR	1.35V power supply of SLDO1
R16	VA12	O	VA12 output voltage
R17	VA12	O	VA12 output voltage
T1	AVSS22_XOBUF	GND	Ground for XO
T2	AVSS22_XO	GND	Ground for XO
T3	AVSS22_XOBUF	GND	Ground for XO
T4	VXO18_LV	PWR	XO IO power
T5	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
T7	AVSS18_AUXADC	GND	AUXADC ground
T8	VTCXO24	O	VTCXO24 output voltage
T9	VCAMA1	O	VCAMA1 output voltage
T10	VFE28	O	VFE28 output voltage
T11	VMCH	O	VMCH output voltage
T12	VEMC	O	VEMC output voltage
T13	VIO28	O	VIO28 output voltage
T14	VCAMD2	O	VCAMD2 output voltage
T15	VS2_SLDO3	PWR	1.35V power supply of SLDO3
T16	VCAMD1	O	VCAMD1 output voltage
T17	VCAMD1_S	O	VCAMD1 output sense
U2	XTAL1	I	XTAL input 1
U3	XTAL2	I	XTAL input 2
U4	AVSS_XO_ISO	GND	XO ISO GND
U5	AUXADC_VIN	I	AUXADC input
U6	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
U7	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock
U8	VCAMA2	O	VCAMD2 output voltage
U10	VBIF28	O	VBIF28 output voltage
U11	VGP	O	VGP output voltage
U12	VSIM1	O	VSIM1 output voltage
U15	VCAMD2_S	O	VCAMD2 output sense
U16	VCAMD1	O	VCAMD1 output voltage

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range				6.0	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

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2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		27.84 [1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

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2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6355 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A1	GND_VS1	0	V
A2	VS1	0~5.0	V
A3	VSYS_VS1	0~5.0	V
A4	VSYS_VPA1	0~5.0	V
A5	VPA1	0~5.0	V
A6	VSYS_VMODEM	0~5.0	V
A7	VMODEM	0~5.0	V
A8	GND_VMODEM	0	V
A9	GND_VPROC1	0	V
A10	VPROC1	0~5.0	V
A11	VSYS_VPROC1	0~5.0	V
A12	VSYS_VPROC2	0~5.0	V
A13	VPROC2	0~5.0	V
A14	GND_VPROC2	0	V
A15	GND_VCORE	0	V
A16	GND_VCORE	0	V
B1	GND_VS1	0	V
B2	VS1	0~5.0	V
B3	VSYS_VS1	0~5.0	V
B7	VMODEM	0~5.0	V
B8	GND_VMODEM	0	V
B9	GND_VPROC1	0	V
B10	VPROC1	0~5.0	V
B11	VSYS_VPROC1	0~5.0	V
B12	VSYS_VPROC2	0~5.0	V
B13	VPROC2	0~5.0	V
B14	GND_VPROC2	0	V
B16	VCORE	0~5.0	V
B17	VCORE	0~5.0	V
C1	GND_VS1	0	V
C6	GND_VPA1	0	V
C16	VSYS_VCORE	0~5.0	V
C17	VSYS_VCORE	0~5.0	V
D1	GND_BUCK_CTRL1	0	V
D2	DVDD12_IO	0~1.98	V
D3	VS1_FB	0~5.0	V
D4	VSYS_BUCK_CTRL1	0~5.0	V
D5	VPA1_FB	0~5.0	V
D6	VMODEM_FB	0~5.0	V
D7	GND_VMODEM_FB	0	V
D9	GND_VPROC1_FB	0	V

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Ball	Symbol	Voltage range	Unit
D10	VPROC1_FB	0~5.0	V
D11	GND_VPROC2_FB	0	V
D12	VPROC2_FB	0~5.0	V
D13	GND_VCORE_FB	0	V
D14	VCORE_FB	0~5.0	V
D16	VSYS_VGPU	0~5.0	V
D17	VSYS_VGPU	0~5.0	V
E2	VS1_SLDO2	0~2.1	V
E3	VIO18	0~2.1	V
E4	VCAMIO	0~2.1	V
E5	VRF18_1	0~2.1	V
E6	VMIPI	0~2.1	V
E7	DVDD18_IO	0~1.98	V
E8	FSOURCE	0 ~ 1.98	V
E9	SPI_CSN	0 ~ 1.98	V
E11	SPI_CLK	0 ~ 1.98	V
E14	VSYS_BUCK_PW	0~5.0	V
E16	VGPU	0~5.0	V
E17	VGPU	0~5.0	V
F1	RTC32K_1V8_1	0 ~ 1.98	V
F3	VUFS18_S	0~2.1	V
F4	VS1_SLDO3	0~2.1	V
F6	VSYS_LDOS4	0~5.0	V
F8	RTC32K_1V8_0	0 ~ 1.98	V
F9	SPI_MISO	0 ~ 1.98	V
F10	SPI_MOSI	0 ~ 1.98	V
F11	AUD_DAT_MISO	0 ~ 1.98	V
F12	SCP_VREQ_VAO	0~1.98	V
F13	GND_VGPU_FB	0	V
F14	VGPU_FB	0~5.0	V
F16	GND_VGPU	0	V
F17	GND_VGPU	0	V
G2	VS1_SLDO1	0~2.1	V
G3	VUFS18	0~2.1	V
G4	VCN18	0~2.1	V
G5	VRF18_2	0~2.1	V
G6	VXO18	0~2.1	V
G8	DVSS18_IO	0	V
G9	GND_LDO	0	V
G10	GND_LDO	0	V
G11	GND_LDO	0	V
G12	GND_LDO	0	V
G13	VOW_CLK_MISO	0~1.98	V
G16	VSYS_VDRAM1	0~5.0	V
G17	VDRAM1	0~5.0	V
H2	AU_V18N	-2.1 ~ 0	V
H4	AU_HPR	-2.1 ~ 2.1	V

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Ball	Symbol	Voltage range	Unit
H5	AU_LOLN	-2.1 ~ 2.1	V
H8	DVSS18_DIG	0	V
H9	GND_LDO	0	V
H10	GND_LDO	0	V
H11	GND_LDO	0	V
H12	AUD_DAT_MOSI	0 ~ 1.98	V
H13	GND_VDRAM_FB1	0	V
H14	VDRAM_FB1	0~5.0	V
H16	GND_VDRAM1	0	V
H17	VSYS_VDRAM2	0~5.0	V
J1	FLYN	-2.1 ~ 0	V
J2	AVSS18_AUD	0	V
J3	AU_HPL	-2.1 ~ 2.1	V
J4	AUDREFN	0	V
J5	AU_LOLP	-2.1 ~ 2.1	V
J6	AU_HSP	-2.1 ~ 2.1	V
J7	AUD_TESTIN	0 ~ 2.1	V
J8	GND_LDO	0	V
J9	GND_LDO	0	V
J10	GND_LDO	0	V
J11	GND_LDO	0	V
J12	AUD_CLK	0 ~ 1.98	V
J14	VDRAM_FB2	0~5.0	V
J16	VDRAM2	0~5.0	V
J17	GND_VDRAM2	0	V
K1	FLYP	0 ~ 2.1	V
K2	AVDD18_AUD	0 ~ 2.1	V
K6	AU_HSN	-2.1 ~ 2.1	V
K7	HOMEKEY	0~1.98	V
K8	WDTRSTB_IN	0 ~ 1.98	V
K9	GND_LDO	0	V
K10	GND_LDO	0	V
K11	GND_LDO	0	V
K12	RESETB	0 ~ 1.98	V
K13	PWRKEY	0~5.0	V
K14	VS2_FB	0~5.0	V
K16	VSYS_VS2	0~5.0	V
K17	VSYS_VS2	0~5.0	V
L2	AVSS30_AUD	0	V
L3	ACCDET	0 ~ 3.3	V
L4	AU_VIN0_P	0 ~ 3.3	V
L5	AU_VIN0_N	0 ~ 3.3	V
L7	AU_MICBIAS0	0 ~ 3.3	V
L8	GND_LDO	0	V
L9	GND_LDO	0	V
L10	GND_LDO	0	V
L11	GND_LDO	0	V

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Ball	Symbol	Voltage range	Unit
L13	UVLO_VTH	0~5.0	V
L14	EXT_PMIC_PG	0~5.0	V
L16	VS2	0~5.0	V
L17	VS2	0~5.0	V
M1	AU_VIN1_N	0 ~ 3.3	V
M2	AU_VIN1_P	0 ~ 3.3	V
M3	AU_VIN2_N	0 ~ 3.3	V
M5	AVDD30_AUD	0 ~ 3.3	V
M6	AU_MICBIAS1	0 ~ 3.3	V
M7	VCDT	0 ~ 3.08	V
M8	CHRLDO	0 ~ 3.08	V
M9	DVSS18_IO_2	0	V
M10	BATADC	0~5.0	V
M11	BATON	0~2.8	V
M12	BATID	0~2.8	V
M13	GND_VREF	0	V
M14	VSRAM_CORE	0~1.4	V
M15	VSRAM_GPU	0~1.4	V
M16	EXT_PMIC_EN	0 ~ 5.0	V
M17	GND_VS2	0	V
N1	AVDD18_CODEC	0 ~ 1.98	V
N2	AU_VIN2_P	0 ~ 3.3	V
N5	AU_MICBIAS2	0 ~ 3.3	V
N6	PMU_TEST_MODE	0~5.0	V
N7	DVDD18_DIG	0~1.98	V
N9	VSYSSNS	0~5.0	V
N10	VSIM2	0~5.0	V
N11	CS_P	-0.1 ~ 0.1	V
N12	CS_N	-0.1 ~ 0.1	V
N13	VREF	0 ~ 1.32	V
N14	VSYS_DRIVER	0~5.0	V
N15	VS2_SLDO2	0~2.1	V
P1	SRCLKEN_IN0	0 ~ 1.98	V
P3	XO_AUD	0.8~1.98	V
P4	XO_SOC	0~1.21	V
P5	SRCLKEN_IN1	0 ~ 1.98	V
P6	RTC32K_2V8	0 ~ 3.08	V
P8	VA18	0~1.98	V
P9	VCN28	0~5.0	V
P10	VUSB33	0~5.0	V
P12	VMC	0~5.0	V
P13	VLDO28	0~5.0	V
P14	VSRAM_MD	0~5.0	V
P15	VSRAM_PROC	0~2.1	V
P16	VA10	0~2.1	V
R1	XO_WCN	0~1.98	V
R2	XO_CEL	0~1.98	V

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Ball	Symbol	Voltage range	Unit
R3	XO_EXT	0~1.98	V
R4	XO_NFC	0~1.98	V
R6	AVDD28_VRTC	0~5.0	V
R7	VGP2	0~5	V
R8	VXO22	0~5	V
R10	VSYS_LDOS1	0~5.0	V
R11	VSYS_LDOS2	0~5.0	V
R12	VCN33	0~5.0	V
R13	VSYS_LDOS3	0~5.0	V
R14	VRF12	0~1.4	V
R15	VS2_SLDO1	0~2.1	V
R16	VA12	0~1.4	V
R17	VA12	0~1.4	V
T1	AVSS22_XOBUF	0	V
T2	AVSS22_XO	0	V
T3	AVSS22_XOBUF	0	V
T4	VXO18_LV	0~1.98	V
T5	AVDD18_AUXADC	0 ~ 1.98	V
T7	AVSS18_AUXADC	0	V
T8	VTCXO24	0~5.0	V
T9	VCAMA1	0~5	V
T10	VFE28	0~5	V
T11	VMCH	0~5.0	V
T12	VEMC	0~5.0	V
T13	VIO28	0~5.0	V
T14	VCAMD2	0~1.4 or 0~2.1	V
T15	VS2_SLDO3	0~2.1	V
T16	VCAMD1	0~2.1	V
T17	VCAMD1_S	0~2.1	V
U2	XTAL1	0~2.2	V
U3	XTAL2	0~2.2	V
U4	AVSS_XO_ISO	0	V
U5	AUXADC_VIN	0~1.98	V
U6	XIN	0 ~ 3.08	V
U7	XOUT	0 ~ 3.08	V
U8	VCAMA2	0~5	V
U10	VBIF28	0~2.8	V
U11	VGP	0~5	V
U12	VSIM1	0~5.0	V
U15	VCAMD2_S	0~1.4 or 0~2.1	V
U16	VCAMD1	0~2.1	V

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2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Ambient temperature (T_A)		-20		85	°C
Junction temperature (T_J)		-20		125	°C

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2.5 Electrical Characteristics

VBAT = 2.7 ~ 5.0V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Standby	Low-power mode		420	480	µA
Power down leakage current with 32K XTAL	VBAT=5.0V, Temp=25°C			85	uA
Under Voltage (UV)					
Under voltage falling threshold (UVLO_VTHL)		2.55	2.6	2.65	V
Threshold voltage accuracy		-50		+50	mV
Under voltage rising threshold (UVLO_VTHH)	R=185K~270K	2.95	3.0	3.05	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		9	11	mA
Delay time from last default on power turn on to RESETB release		64	80	96	ms
PWRKEY					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time		29.6	37	44.4	ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.75*VIO			V
Control input low (SPI, SRCLKEN related)				0.25*VIO	V
Thermal Shut-down					
PMIC shut-down threshold		135	150	165	degree
Shut-down release threshold		95	110	125	degree

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2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VDRAM1					
Turn-on overshoot	Vout=1.125V No load Cout=66uF			10	%
Short current		2000		2500	mA
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/Full Imax	-100		+100	ppm/°C
Efficiency	Vbat=4V, Vout=1.125V, L_DCR=50mΩ I_Load=100mA		89		%
	Vbat=4V, Vout=1.125V, L_DCR=50mΩ I_Load=500mA		85		%
	Vbat=4V, Vout=1.125V, L_DCR=50mΩ I_Load=1.0A		81		%
	Vbat=4V, Vout=1.125V, L_DCR=50mΩ I_Load=1.7A		75		%
Soft start	Vout=1.125V No load Cout=66uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			1	%
Load transient (PFM to PWM)	Vbat=3.8V IOUT=0A to 800mA (Tr/Tf=0.9us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 5.0V I_Load= transient point to Imax	-1.1		+1.1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 5.0V I_Load=0A ~ transient point	-1.6		+3	%
Buck – VDRAM2					
Turn-on overshoot	Vout=0.6V No load Cout=44uF			10	%
Short current		1000		1500	mA
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/Full Imax	-100		+100	ppm/°C
Efficiency	Vbat=4V, Vout=0.6V, L_DCR=50mΩ I_Load=50mA		79		%
	Vbat=4V, Vout=0.6V, L_DCR=50mΩ I_Load=100mA		79		%
	Vbat=4V, Vout=0.6V,		80		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR=50mΩ I_Load=200mA				
	Vbat=4V, Vout=0.6V, L_DCR=50mΩ I_Load=550mA		70		%
Soft start	Vout=0.6V No load Cout=44uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			1	%
Load transient (PFM to PWM)	Vbat=3.8V IOUT=0A to 350mA (Tr/Tf=1.17us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 5.0V I_Load= transient point to Imax	-1.1		+1.1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 5.0V I_Load=0A ~ transient point	-1.6		+3	%
Buck – VCORE					
Turn-on overshoot	Vout=0.6V No load Cout=44uF			10	%
Short current		Imax*1.2		Imax*1.5	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax			100	ppm/ °C
Efficiency	Vbat=4V, Vout=0.6V, L_DCR=30mΩ I_Load=100mA		83		%
	Vbat=4V, Vout=0.6V, L_DCR=30mΩ I_Load=500mA		83		%
	Vbat=4V, Vout=0.6V, L_DCR=30mΩ I_Load=1.0A		74.5		%
	Vbat=4V, Vout=0.6V, L_DCR=30mΩ I_Load=3A		61.9		%
Soft start	Vout=0.6V No load Cout=44uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp
Load transient (PWM)	Vbat=3.8V IOUT=1.5A to 4A (Tr/Tf=1us)	-4		+4	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 5.0V I_Load=mode change level to Imax	-1.6		+1.6	%
DC accuracy (Included Line/Load regulation	VBAT=2.8V to 5.0V I_Load=0A ~ mode change	-1.6		+15mV	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
@PFM)	level				
Buck – VPROC					
Turn-on overshoot	Vout=0.75V No load Cout=44uF/phase			10	%
Short current		Imax*1.2		Imax*1.5	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax			100	ppm/ °C
Efficiency	Vbat=4V, Vout=0.75V, 2phase L_DCR=30mΩ I_Load=500mA		83.5		%
	Vbat=4V, Vout=0.75V, 2phase L_DCR=30mΩ I_Load=1.0A		77		%
	Vbat=4V, Vout=0.75V, 2phase L_DCR=30mΩ I_Load=2.0A		77.5		%
	Vbat=4V, Vout=0.75V, 2phase L_DCR=30mΩ I_Load=8A		60		%
Soft start	Vout=0.75V No load Cout=44uF/phase			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 2.3A to 4.9A (Tr/Tf = 1us)	-4		+4	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 5.0V I_Load=mode change level to Imax	-1.6		+1.6	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 5.0V I_Load=0A ~ mode change level	-1.6		+15mV	%
Buck – VGPU					
Turn-on overshoot	Vout=0.85V No load Cout=44uF			10	%
Short current		Imax*1.2		Imax*1.5	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax			100	ppm/ °C
Efficiency	Vbat=4V, Vout=0.85V, L_DCR=30mΩ I_Load=100mA		86		%
	Vbat=4V, Vout=0.85V, L_DCR=30mΩ I_Load=500mA		85.6		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	Vbat=4V, Vout=0.85V, L_DCR=30mΩ I_Load=1.0A		79.8		%
	Vbat=4V, Vout=0.85V, L_DCR=30mΩ I_Load=3A		69.2		%
Soft start	Vout=0.85V No load Cout=44uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 0.5A to 2.3A (Tr/Tf = 1us)	-4		+4	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 5.0V I_Load=mode change level to Imax	-1.6		+1.6	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 5.0V I_Load=0A ~ mode change level	-1.6		+15mV	%
Buck – VMODEM					
Turn-on overshoot	Vout=0.8V, VBAT=3.8V No load Cout=66uF			10	%
Short current		Imax*1.2		Imax*3	A
Temperature coefficient	Vbat=3.8V PWM Mode * Compare with 25C	-1		1	%
Efficiency	Vbat=4V, Vout=0.8V, L_DCR=30mΩ I_Load=400mA		86		%
	Vbat=4V, Vout=0.8V, L_DCR=30mΩ I_Load=850mA		82		%
	Vbat=4V, Vout=0.8V L_DCR=30mΩ I_Load=2.1A		69		%
Soft start	Vout=0.8V No load Cout=66uF			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			10	mVpp
Load transient (PWM)	Vbat=3.8V, Vout=0.8V IOUT=0.8A to 1.6A (Tr/Tf=1us)	-4.7		+5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 5.0V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 5.0V Vout=0.8V I_Load=0~10mA	-1		1% + 31mV	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VPA					
Turn-on overshoot	Vo=0.5V Vo=3.4V			15 10	%
Short current	a. 0.6 ≥ Vo > 0.5V b. 1.25 ≥ Vo > 0.7V c. 2.5 ≥ Vo > 1.3V d. 3.6 ≥ Vo > 2.6V		a. 0.8 b. 1.0 c. 2.2 d. 3.2		A
Temperature coefficient	Vbat=3.8V Load=PWM,Vo=3.4V	-1		+1	%
Efficiency	Vbat=3.8V, Vout=0.5V, L_DCR < 55mΩ I_load=40mA		75		%
	Vbat=3.8V, Vout=1.2V, L_DCR < 55mΩ I_oad=200mA		84		%
	Vbat=3.8V, Vout=2.4V, L_DCR < 55mΩ Ioad=400mA		91		%
	Vbat=3.8V, Vout=3.4V, L_DCR < 55mΩ Ioad=650mA		94		%
	Vbat=3.8V, Vout=3.4V, L_DCR < 55mΩ Ioad=800mA		92		%
Soft start	No load			300	us
Output Ripple Voltage (PWM)	Vbat=3.8V @25°C I_Load=0.5*Imax 20MHz measurement BW			50	mVpp
	0.7V > (Vbat-Vout) > 0.2V I_Load=0.5*Imax 20MHz measurement BW			100	mVpp
Load transient	Vbat=3.8V, Vout=3.4V ILOAD=50mA <-> 800mA (Tr/Tf=1.6us)			400	mV
DC accuracy	Vout=0.5~1V @25°C VBAT=3.8V I_load=PWM	-20		+20	mV
	VBAT=3.8V VBAT– Vout ≥ 400mV; Vout ≥ 1V Iload=PWM	-2		+2	%
Buck – VS1					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/Full Imax	-100		+100	ppm/ °C
Efficiency	Vbat=4V, Vout=2V, L_DCR=53mΩ I_Load=50mA		90		%
	Vbat=4V, Vout=2V, L_DCR=53mΩ		90		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	I_Load=500mA				
	Vbat=4V, Vout=2V, L_DCR=53mΩ I_Load=1 A		87		%
	Vbat=4V, Vout=2V L_DCR=53mΩ I_Load=3.5A		70		%
Soft start	No load			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			0.6	%p-p
Load transient (PWM)	Vbat=3.8V IOUT=2.5A to 3.5A (Tr/Tf=5us)	-4		+5.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 5.0V I_Load= transient point to Imax	-2.15		+2.15	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 5.0V I_Load=0~ transient point	-0.9		+4.1	%
Buck – VS2					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/Full Imax	-100		+100	ppm/ °C
Efficiency	Vbat=3.8V, Vout=1.35V, L_DCR=53mΩ I_Load=50mA		84		%
	Vbat=3.8V, Vout=1.35V, L_DCR=53mΩ I_Load=500mA		89		%
	Vbat=3.8V, Vout=1.35V, L_DCR=53mΩ I_Load=1A		83		%
	Vbat=3.8V, Vout=1.35V, L_DCR=53mΩ I_Load=3A		66		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			0.6	%
Load transient (PWM)	Vbat=3.8V IOUT=1.2A to 2.2A (Tr/Tf=5us)	-4.5		+5.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 5.0V I_Load= transient point to Imax	-1.9		+1.9	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 5.0V I_Load=0~ transient point	-0.9		+6	%

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Table 2-6. LDO specifications

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
Power source	ALDO and DLDO	VBAT voltage		max{Vo+0.35 ; 3.15}		5	V
	SLDO1 and SLDO2	VBAT voltage		3.15		5	V
	SLDO1	VS1=2.0V		max{Vo+0.15 ; 2*0.95}		2*1.05	V
	SLDO2	VS2=1.35V		max{Vo+0.1 ; 1.35*0.95}		1.35*1.05	V
Overall DC voltage accuracy	ALDO, DLDO and SLDO Normal mode	Default voltage		-1.5		+1.5	%
		Non default voltage		-3		+3	%
	ALDO, DLDO and SLDO Low power mode	All voltages		-4		+4	%
Load regulation	ALDO, DLDO and SLDO Normal mode	Iout = 0mA~Imax	1. Power source 2. Typical capacitor 3. TA= -40°C ~ +85°C	-1.5		+1.5	%
	ALDO, DLDO and SLDO Low power mode	Iout= 0mA~5mA		-4		+4	%
	VRTC,DVDD18_DIG	Iout = 0mA~0.2*Imax		-10		+10	%
Line regulation	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C	-1.5		+1.5	%
	VRTC,DVDD18_DIG	Iout = 0mA		-5		5	%
Power off voltage	ALDO, DLDO and SLDO	Iou t= 0mA	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C			0.2	V
Load transient response	ALDO	Iout = 1mA~0.5*Imax @ Slew rate = 15mA/us	1. Power source 2. Typical capacitor 3. TA= -40°C ~+85°C	-4		+4	%
	DLDO and SLDO	Iout = 1mA~0.5*Imax @ Slew rate = 80mA/us					
Turn-on rise time	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			300	us

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Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
Turn-on overshoot	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			+10	%
Normal mode quiescent current	ALDO	Iout = 0mA	1. Power source 2. Typical capacitor 3. TA= 25°C			55	uA
	DLDO					55	
	SLDO (Current loading ≦ 0.3A)					100	
	SLDO (0.3A<Current loading≦ 0.6A)					160	
	SLDO (Current loading > 0.6A)					220	
	VRTC and DVDD18_DIG					10	
Low power mode quiescent current	SLDO					15	
	ALDO, DLDO					10	
Power off time	ALDO, DLDO and SLDO	Iout = 0mA	1. Power source 2. Capacitor ≦ 2.2uF 3. TA= 25°C			4	ms
			1. Power source 2. Capacitor ≦ 9.4uF 3. TA= 25°C			12	ms
Output noise	ALDO	Freq = 10Hz to 80kHz	1. Power source 2. Typical capacitor 3. TA= +25°C 4. Iout = 0.2*Imax~0.5*Imax		90		uVrms
	DLDO and SLDO				500		uVrms
	ALDO, DLDO and SLDO	Freq = 10Hz to 10MHz			1000		uVrms
PSRR	ALDO	Freq = 217Hz to 3kHz	1. Power source 2. Typical capacitor 3. TA= +25°C 4. Iout = 0.2*Imax~0.5*Imax		65		dB
		Freq= 3kHz to 30kHz			45		dB
	DLDO and SLDO	Freq = 217Hz			40		dB
Short current	Imax ≦0.5A	OC	1. Power source 2. Typical capacitor 3. TA= +25°C	max{Imax* 1.2 ; 0.05}		1.5	A
		OCFB		0.02		0.8	A
	Imax > 0.5A	OC		max{Imax*		3.6	A

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Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
				1.2 ; 0.7}			
		OCFB		0.1		2.4	A

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2.7 Charger-In Detection

Table 2-7. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
VCDT CHRIN UVLO rising detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4.2		4.45	V
	Accuracy (Default CHRIN=4.3V)	-3%	4.3	3%	
VCDT CHRIN UVLO falling detection threshold	Falling level for charger plug-out detection (default)		3.9		V
	Programmable	2.8		3.9	
	Accuracy	-6%		6%	
VCDT CHRIN OVP detection threshold	VCDT_VTHH[7:4] = 0000 ~ 1111	6		14	V

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2.8 Audio CODEC

Table 2-8. Audio downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Headphone Output (Single-ended Output, AU_HPL/R; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +7dB, 24bit audio data					
P_{OUT}	Maximum output power @<0.1% THD		33.8		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		111		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -91 -93 -95		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -91 -93 -95		dB
NF_{OUT}	Output Noise Floor (A-weighted)		2.65		µVrms (A)
R_{LOAD}	Output Resistor Load (headphone)	16	32		Ω
C_{LOAD}	Output Capacitor Load			250	pF
$APGR_{DL}$	Analog Programmable Gain Range	-22		8	dB
$APGS_{DL}$	Analog Programmable Gain Step		1		dB
XT_{LR}	L/R Channel Separation @ 1kHz		-110		dB
PSRR	Power Supply Rejection Ratio (from AVDD18_AUD to AU_HPL/R)		-100		dB
DAC to Headphone Output (Single-ended Output, AU_HPL/R; R_{LOAD} = 16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +4dB, 24bit audio data					
P_{OUT}	Maximum output power @<0.1% THD		41.5		mW
SNR (1)	Signal to Noise Ratio (A-weighted)		108		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 22.5mW		 -90 -93		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 22.5mW		 -90 -93		dB
NF_{OUT}	Output Noise Floor (A-weighted)		2.5		µVrms (A)

Note1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

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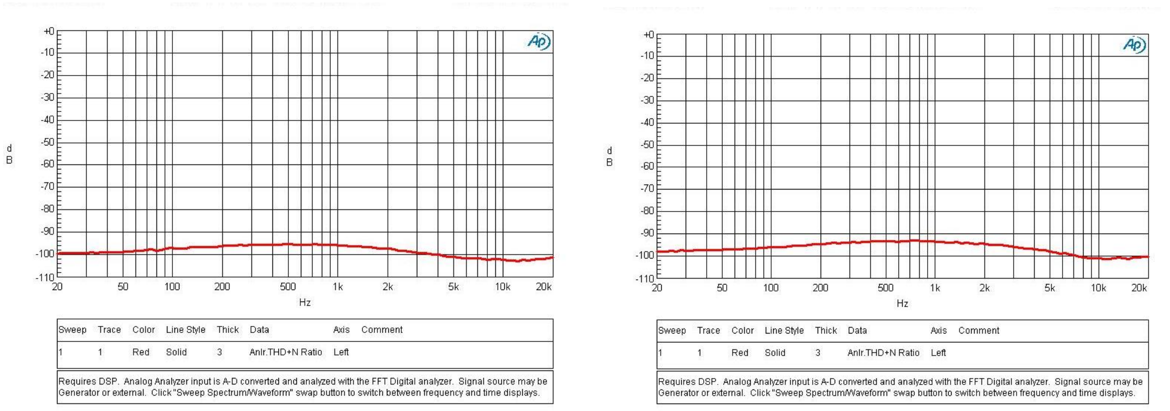
Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Headset Output (Differential Outputs, AU_HSP/N; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +8dB, 24bit audio data					
P_{OUT}	Maximum output power @<1% THD		137		mW
SNR (1)	Signal to noise ratio (A-weighted)		-111		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -90 -90		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -90 -90		dB
NF_{OUT}	Output noise floor (A-weighted)		4.9		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
PSRR	Power supply rejection ratio (from AVDD18_AUD to AU_HSP/N)		-100		dB
DAC to Headset Output (Differential Outputs, AU_HSP/N; R_{LOAD} =16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +6dB, 24bit audio data					
P_{OUT}	Maximum output power @<1% THD		157		mW
SNR (1)	Signal to noise ratio (A-weighted)		-109		dB(A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -85 -85		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -85 -85		dB
NF_{OUT}	Output noise floor (A-weighted)		4.3		µVrms (A)

Note1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer



(a) P_{OUT}=22.5mW (b) Pout=10mW

Figure 2-1. Audio path THD+N vs. frequency

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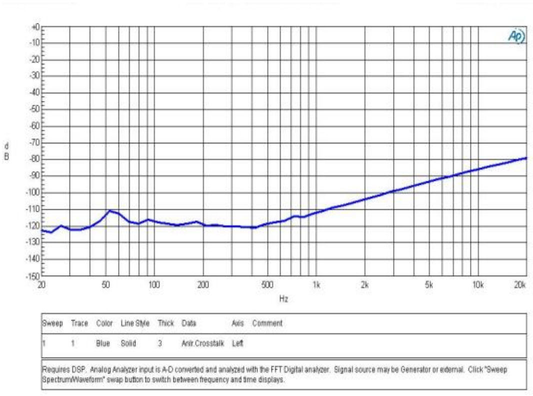
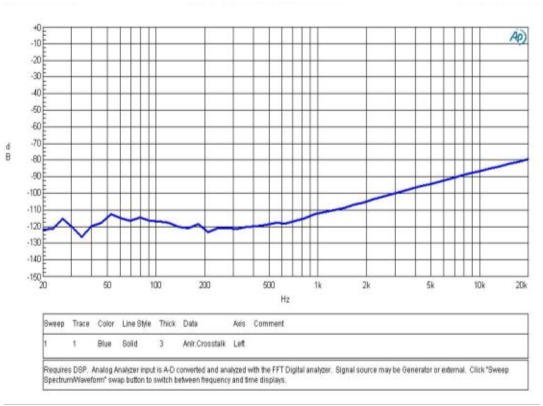


(a) Xtalk RtoL



(b) Xtalk LtoR

Figure 2-2. Audio path Xtalk vs. frequency @P_{OUT}=10mW

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Line-out Output (Differential Outputs, AU_LOLP/N; R_{LOAD} = 560) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, PGA_{DL} gain = +8dB, 24bit audio data					
P_{OUT}	Maximum output swing @<1% THD @PGA_{DL} gain =+8dB gain		6.86		dBV
SNR (1)	Signal to noise ratio (A-weighted)		-111		dB (A)
THD	Total Harmonic Distortion (THD) @P_{OUT} = 6.8mW		-90		dB
THD+N	THD Plus Noise (THD+N) @P_{OUT} = 6.8mW		-90		dB
NF_{OUT}	Output noise floor (A-weighted)		4.48		µVrms (A)
R_{LOAD}	Output resistor load (headphone)		600		Ω
C_{LOAD}	Output capacitor load			500	pF
$APGR_{DL}$	Analog programmable gain range	-10		8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
PSRR	Power supply rejection ratio (from AVDD18_AUD to AU_LOLP/N)		-100		dB

Note1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Table 2-9. Audio uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue Input Paths to ADC (Differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		97		dB
N_{IN}	Input-referred noise		14		µVrms
THD	Total Harmonic Distortion (THD) @0dBV(-3dBFS) input		-90		dB
THD+N	THD Plus Noise (THD+N) @0dBV(-3dBFS) input		-88		dB
	THD Plus Noise (THD+N) @-60dBV(-63dBFS) input		-37		dB
Analogue Input Paths to ADC (Differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		90		dB
N_{IN}	Input-referred noise		4.4		µVrms

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Symbol	Parameter	Min.	Typ.	Max.	Unit
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-86		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-30		dB
Analogue Input Paths to ADC (Differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		98		dB
N_{IN}	Input-referred noise		14		µVrms
THD	Total Harmonic Distortion (THD) @0dBV(-3dBFS) input		-90		dB
THD+N	THD Plus Noise (THD+N) @0dBV(-3dBFS) input		-88		dB
	THD Plus Noise (THD+N) @-60dBV(-63dBFS) input		-38		dB
Analogue Input Paths to ADC (Differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		91		dB
N_{IN}	Input-referred noise		4		µVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-90		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-86		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-31		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured w/i A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The input voltage range of AU_VIN0, AU_VIN1, and AU_VIN2 are within [AVDD30_AUD, AVSS30_AUD], and the suggested maximum input swing Vpp ≤ 1Vrms (0 dBV) @ PGA_{UL} gain = 0dB

General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
$APGR_{UL}$	Uplink analog programmable gain range	0		24	dB
$APGS_{UL}$	Uplink analog programmable gain step		6		dB
CMRR	Common-mode rejection ratio @-18dBV, 1kHz sinusoid signal to both pins of an input configured differentially	40	75		dB
XT_{TALK}	ULL-to-ULR channel separation @ one input terminated with -18dBV, 1KHz sinusoid signal. Measure digital output of terminated channel	60	100		dB
XT_{DL2UL}	DL-to-UL channel separation @ 0dBV, 1kHz Rx path with RLOAD = 32	60	105		dB
PSRR	217Hz @ 200 mVpp square wave imposed on power. Measure digital output		80		dB
	1kHz @ 200 mVpp square wave imposed on power. Measure digital output		81		dB
	10kHz @ 200 mVpp square wave imposed on power. Measure digital output		82		dB
$F_{S,UL}$	Audio uplink sampling rate 8, 16, 32, 48	8		48	KHz

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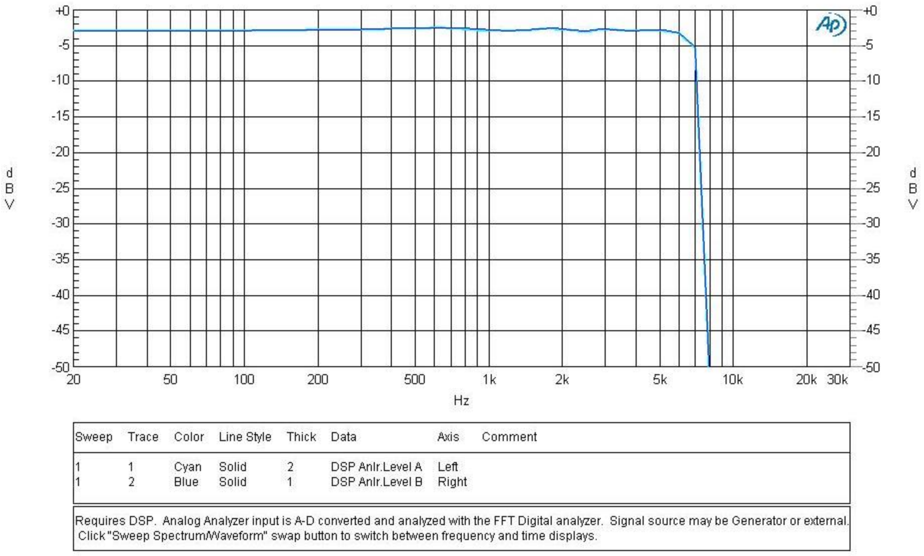

Figure 2-3. Frequency response ($F_{S,UL}$ = 16kHz)

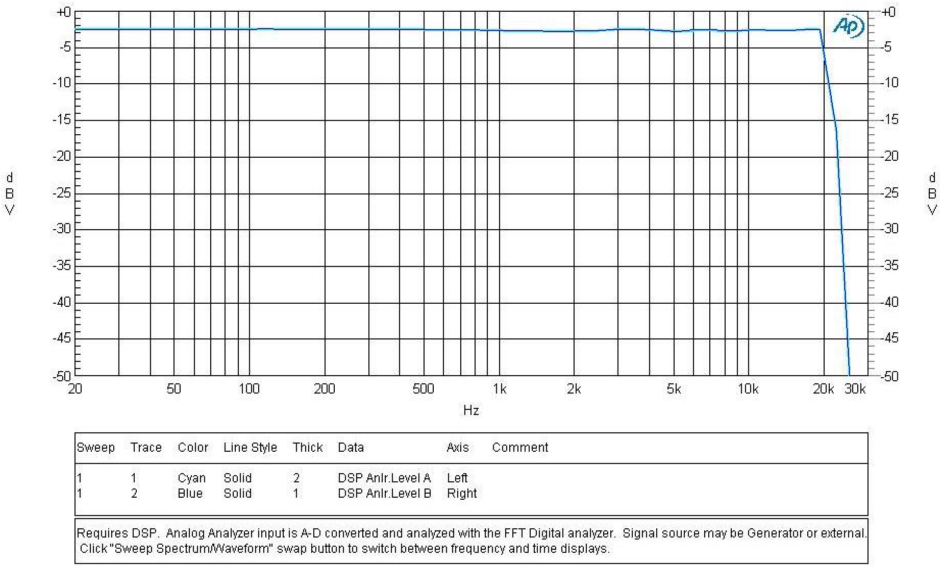

Figure 2-4. Frequency response ($F_{S,UL}$ = 48kHz)

Digital MIC					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
DCLK	DMIC clock frequency	0.514	3.25/1.62	4.33	MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns

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Table 2-10. MICBIAS specifications

Microphone Bias (MICBIAS) Temp = 25deg, 1µF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT}	Microphone bias voltage	1.7		2.7	V
V_{OUT} Step	Bias voltage output step size 1.7~2.1 2.5~2.7		0.1		V
I_{OUT}	Maximum output current (two MICBIAS loads total)			3	mA
N_{OUT}	Output integrated noise (20~20kHz A-weighted) with 1µF cap @ V_{OUT} = 2.7V.		4.7		µVrms
PSRR	217Hz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
	1kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		110		dB
	10kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		100		dB
$C_{LOAD,MIC}$	Output Capacitor Load on MICBIAS	0.1		22	µF

Table 2-11. ACCDET specifications

Accessory Detection (ACCDET)					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
-	*1: Load impedance detection range (ACCDET) by 1 & 1.5kΩ (1%) MICBIAS resistors. *2: The characteristics assume no other component is connected to ACCDET. *3: The key detection voltage will be normalized automatically. For different micbias settings, the same key (resistance is the same) is pressed, and the read voltage (key pressed) value will be similar.				
-	4-pole microphone detection	2K		14K	Ω
-	Microphone impedance detection after 4-pole microphone plugged-in				
-	MICD_LVL[0]: Down key	400		620	Ω
-	MICD_LVL[1]: Up key	150		320	Ω
	MICD_LVL[2]: Hook key	0		100	Ω

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2.9 AUXADC

Table 2-12. AUXADC specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Supply voltage		1.7	1.8	1.9	V
Resolution	AUXADC_VIN			15	Bits
	Others			12	Bits
Analog-input bandwidth			50K		Hz
Sample rate			100K		Hz
Offset error	Relative to full-scale	-1		+1	%
Gain error	Relative to full-scale	-1		+1	%
INL	15-bit output	-2		+2	LSB
DNL	15-bit output	-2		+2	LSB
Current consumption			350		uA

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2.10 Fuel Gauge

Table 2-13. Fuel gauge specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/2		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		1.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

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2.11 BIF

Table 2-14. BIF specifications

Parameter	Description	Unit	Min.	Typ.	Max.
VIH	V input high (voltage level at input, which will be interpreted as high).	V	0.9		
VIL	V input low (voltage level at input, which will be interpreted as low.	V			0.3
VOH	V Output High.	V	1.1		2.8
VOL	When output is low, circuitry will draw BCL voltage lower than VOL voltage, measured from the output.	V	-0.3		0.1

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2.12 XO

Table 2-15. XO specification

Parameter	Test condition	Title	Unit	Min.	Typ.	Max.
Supply current in suspend (OSC LPM)	VXO22 =2.2V; without 32K RTC	$I_{xo,lpm}$	uA		75	
Supply current in idle (OSC + XO_SOC)	VXO22 =2.2V; Cload < 20pF	$I_{xo,idle}$	mA		0.54	
	VXO18 =1.8V; Cload < 20pF				1	
Supply current in RF TRx (OSC + XO_SOC, XO_CEL)	VXO22 =2.2V; Cload < 20pF	$I_{xo,trx}$	mA		3.8	
	VXO18 =1.8V; Cload<20pF				1	
Extra supply current for XO_WCN	VXO22 =2.2V; Cload < 20pF	$I_{xo,conn}$	mA		2	
Extra supply current for one of XO_NFC/XO_EXT/XO_AUD	VXO18 =1.8V; Cload < 20pF	$I_{xo,buffer}$	mA		1	
Leakage current	VXO22 =2.2V; with 32K RTC	$I_{xo,leak}$	uA			1
Center operating frequency	Internal resonant; with QVL crystal	F_{xo}	MHz		26	
Duty cycle	Square wave in high driving mode		%	45	50	55
XO_CEL/XO_WCN Voltage Swing	Square wave in high driving mode; Cload < 30pF		Vpp	1.62	1.8	1.98
XO_SOC/XO_NFC/XO_AUD/XO_EXT voltage swing	Square wave in high driving mode; Cload < 30pF (XO_PD Cload < 50pF)		Vpp	0.8	1.1	1.3
Static tuning range	XTAL1/2 differential input capacitance	C_{TR}	pF	4.0		8.5
CapID binary bits	CDAC		bit		8	
Startup time, after clock request	Delta f < 1ppm.	$T_{startup}$	ms		1	2
Crystal input pins	Specific foundries		pin		2	

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3 Functional Descriptions

3.1 General Descriptions

MT6355 is a fully integrated PMIC target for smart phone power provider. Figure 3-1. is the block diagram of MT6355 PMIC.

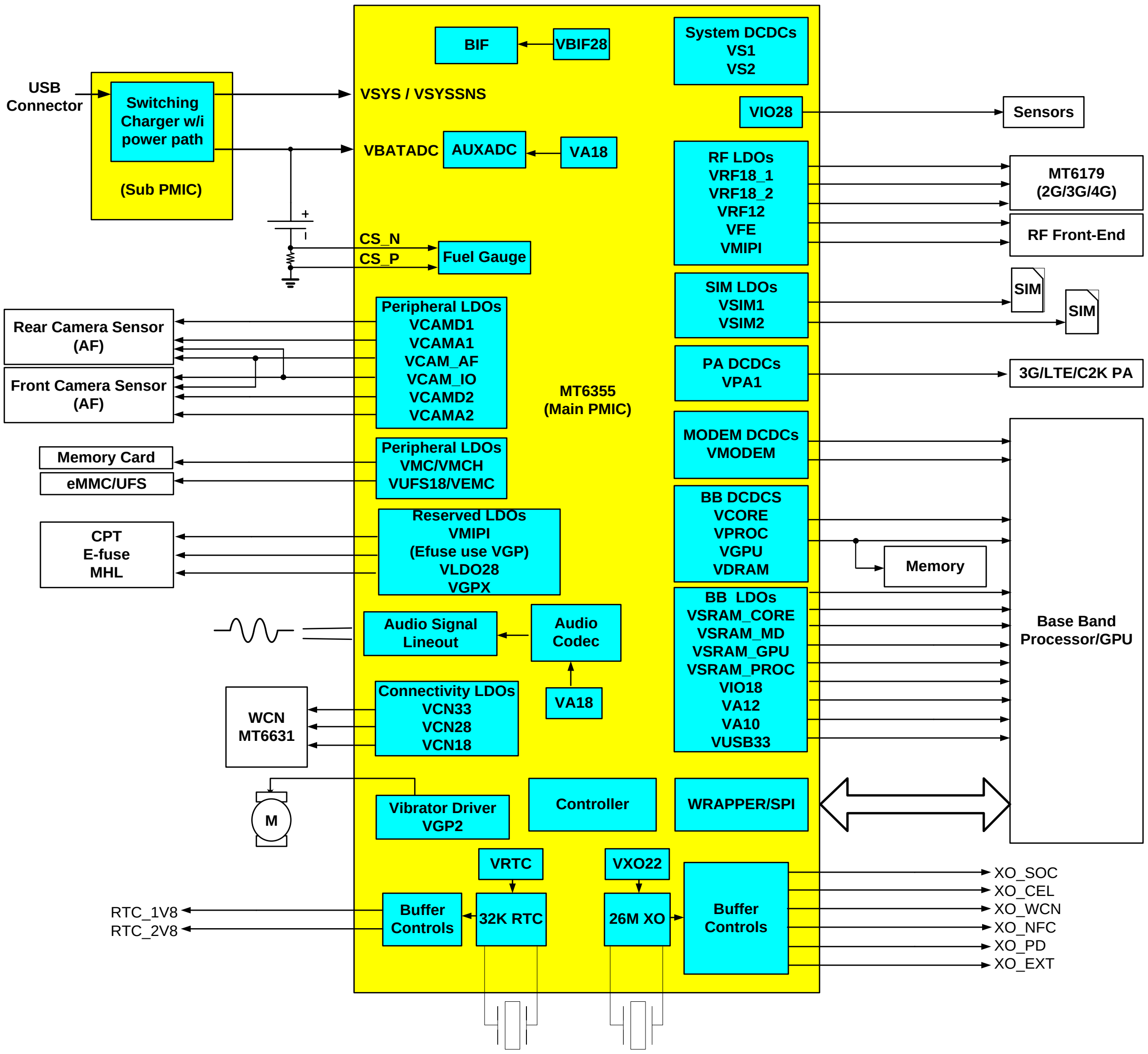

Figure 3-1. MT6355 block diagram

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3.2 PMIC Functional Blocks

MT6355 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6355 includes the following analog functions for use on smart phone platforms.

- LDO and BUCK: Provides regulated lower output voltage level directly from Li-Ion battery or from Li-Ion battery through power path of switching charger with power path management.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- XO: 26MHz oscillator with external Temperature Sensing Xtal (TSX) only.
- BIF: Provides smart battery related functions.
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. ***The power on sequence can be modified by efuse. The power off sequence can be modified by register***. If the battery voltage is neither in the UVLO state (VBAT ≥ UVLO_VTHH) nor in the thermal condition, there are four methods to power on the handset system.

1) Pulling PWRKEY low (user presses PWRKEY.)
2) Valid charger plug-in
3) ALARM
4) SPAR

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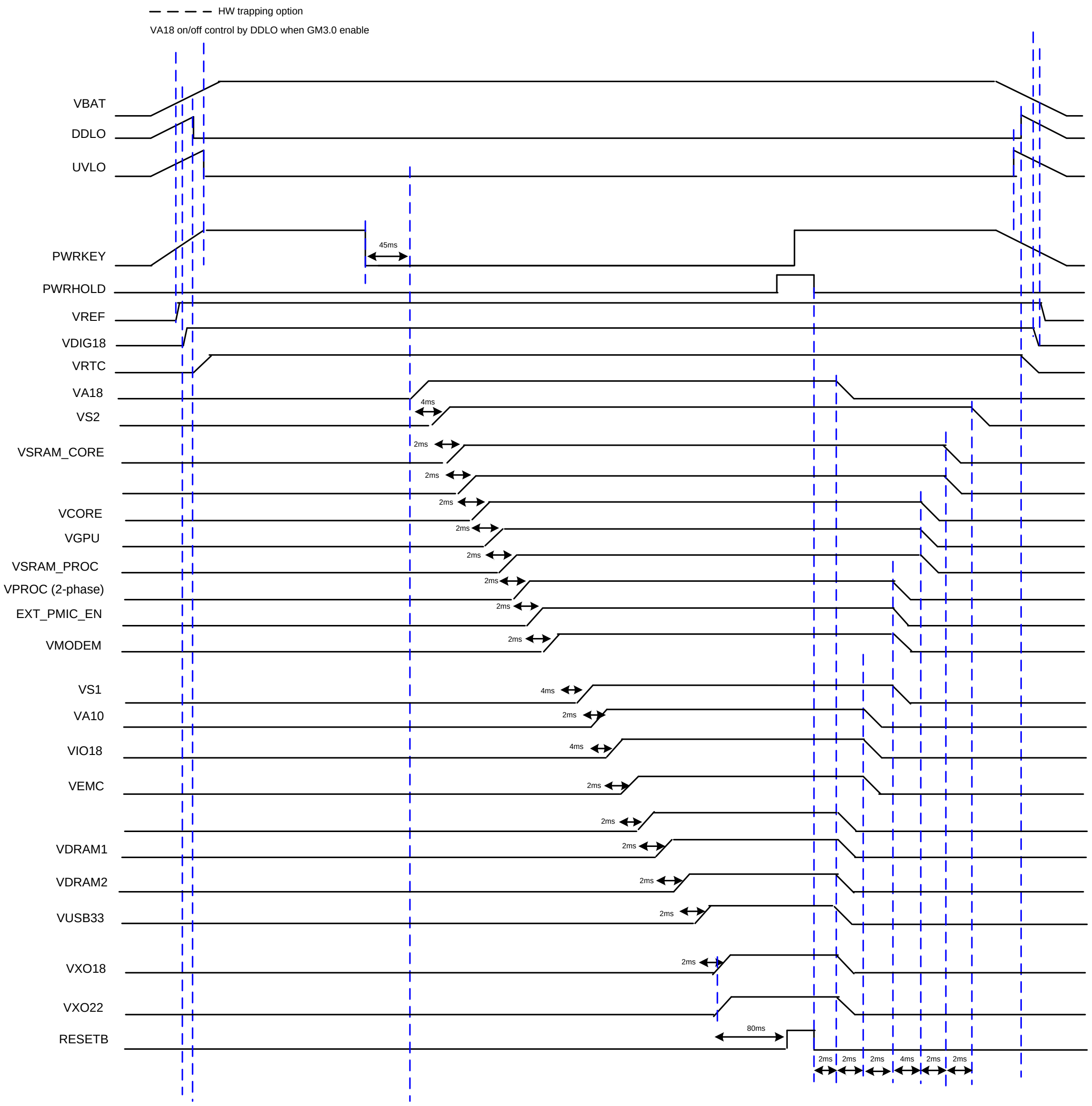

Figure 3-2. Power-on/off control sequence with XTAL by pressing PWRKEY

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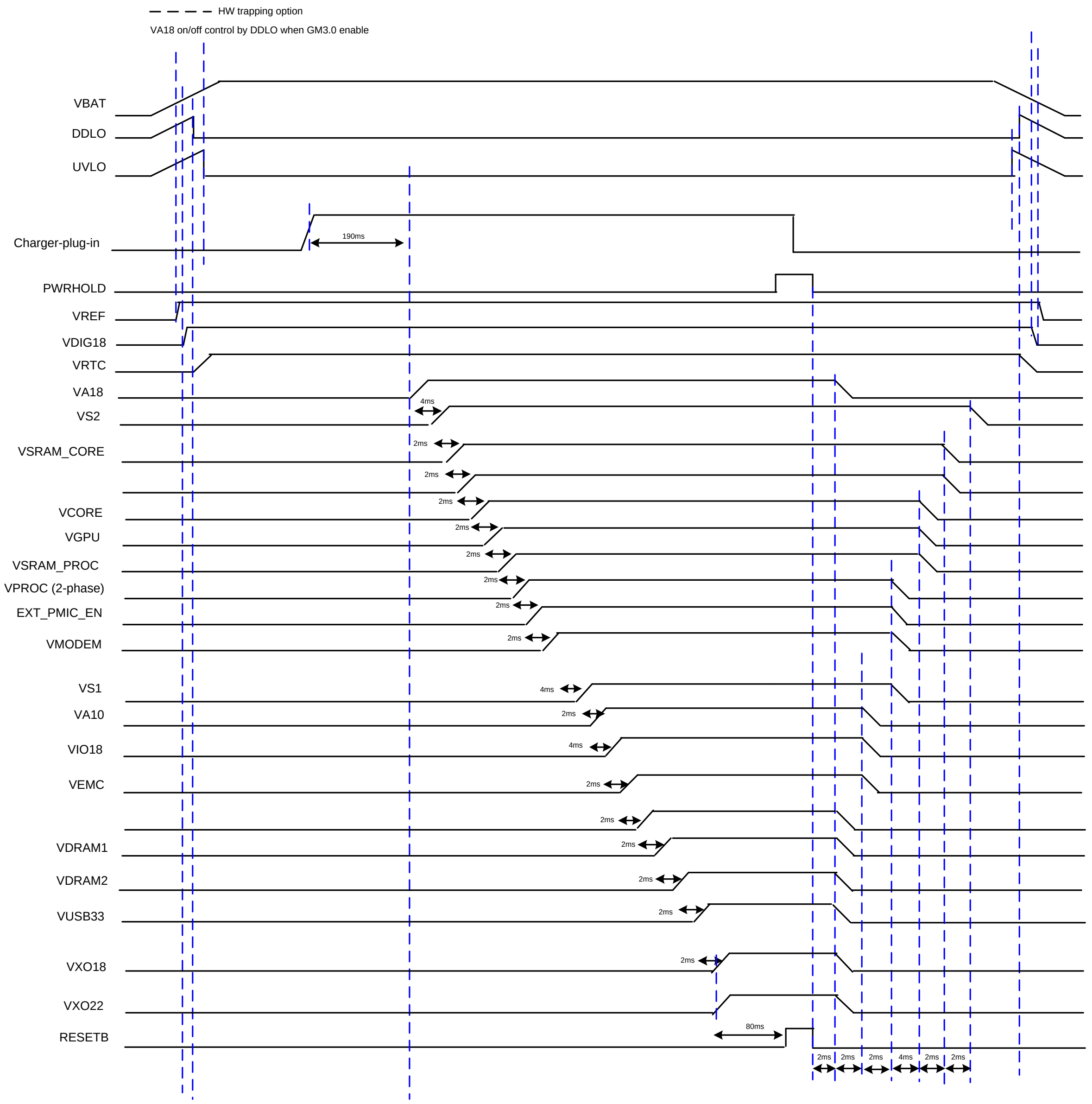

Figure 3-3. Power-on/off control sequence with XTAL by charger plug in

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the PWRHOLD signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives PWRHOLD from the baseband.

2. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage is inside valid range between CHGIN_VTHL and CHGIN_VTHH and VSYS>UVLO, the handset will also be powered on. For gauge function, VBIF28 will auto turned on when the

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charger is plugged in and VSYS > DDLO.

3. RTC module generates ALARM to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the ALARM signal will be directly sent to PMIC. In this case, ALARM becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

4. RTC module generates SPAR to power on the system. When the sudden power drops less than the pre-defined time period during system on and the VSYS back to above UVLO, SPAR is held high to allow PMIC to power on.

Under-voltage lockout (UVLO)
The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VSYSNS. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)
PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset
PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection
If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are eight buck converters in MT6355 to efficiently generate regulated power for graphic processor, digital core and circuits. The block diagram is shown in Figure 3-1. The buck converters operate with 2.57 or 2MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that

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the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 3-1. Buck converter brief specifications

(Default voltage is set by e-fuse for different platforms.)

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VPROC (2 phase BUCK)	0.85	0.45~1.2V	6.25	10000	Y	Processor
VGPU	0.8	0.45~1.1V	6.25	3000	Y	GPU
VCORE	0.8	0.45~1.1V	6.25	4000	Y	CORE_AO
VMODEM	0.8	0.45~1.1V	6.25	2100	Y	BB1 &BB2(LTE) & AP MCU
VS1	2	1.86~2.2V	12.5	3500	Y	System LDO
VS2	1.35	1.25~1.5V	12.5	3000	Y	System LDO
VDRAM1	1.225/1.125	1.225/1.125	6.25	1700	Y	LPDDR3/LPDDR4
VDRAM2	0.6	0.6	6.25	550	Y	LP4X
VPA	0.5	0.5~3.6	50	1000	N	3G/ LTE PA

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

(Default voltage is set by e-fuse for different platforms.)

Type	LDO name	Input power domain	Default voltage (V)	Iout (mA)	Application category
ALDO	VFE28	VSYS_LDOS1	2.8	40	RF AFE
ALDO	VTCXO24	VSYS_LDOS1	2.375	40	DCXO
ALDO	VXO22	VSYSSNS or BATSNS	2.2	40	DCXO
SLDO1	VXO18	VSYS_LDOS4 and VS1_SLDO3	1.81	20	DCXO
SLDO1	VRF18_1	VSYS_LDOS4 and VS1_SLDO3	1.81	450	RF IC (MT61 77L)
SLDO1	VRF18_2	VSYS_LDOS4 and VS1_SLDO3	1.81	450	RF IC (MT6177L)
SLDO2	VRF12	VSYS_LDOS3 and VS2_SLDO1	1.2	400	RF IC (MT6177L)
DLDO	VCN33	VSYS_LDOS3	3.3	800	Connectivity
ALDO	VCN28	VSYS_LDOS1	2.8	40	Connectivity
SLDO1	VCN18	VSYS_LDOS4 and VS1_SLDO3	1.8	200	Connectivity
ALDO	VCAMA1	VSYS_LDOS1	2.8	125	Camera analog power
ALDO	VCAMA2	VSYS_LDOS1	2.8	110	Camera analog power

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Type	LDO name	Input power domain	Default voltage (V)	Iout (mA)	Application category
SLDO1	VCAMIO	VSYS_LDOS4 and VS1_SLDO3	1.8	140	Camera IO power
SLDO2	VCAMD1	VSYS_LDOS3 and VS2_SLDO1	1.2	500	Main Camera digital power
SLDO1	VCAMD2	VSYS_LDOS3 and VS2_SLDO3	1.2	500	Main Camera digital power
SLDO2	VA10	VSYS_LDOS3 and VS2_SLDO1	0.9	250	AP Analog module
SLDO2	VA12	VSYS_LDOS3 and VS2_SLDO1	1.2	500	AP Analog module
ALDO	VA18	VSYSSNS or BATSNS	1.8	40	Audio + AuxADC
SLDO2	VSRAM_PROC	VSYS_LDOS3 and VS2_SLDO2	0.95	600	CPU SRAM
SLDO2	VSRAM_GPU	VSYS_LDOS3 and VS2_SLDO2	0.95	200	GPU SRAM
SLDO2	VSRAM_MD	VSYS_LDOS3 and VS2_SLDO2	0.9	300	MODEM SRAM
SLDO2	VSRAM_CORE	VSYS_LDOS3 and VS2_SLDO2	0.9	300	Core SRAM
DLDO	VSIM1	VSYS_LDOS2	1.86	100	SIM card
DLDO	VSIM2	VSYS_LDOS2	1.86	100	SIM card
DLDO	VLDO28	VSYS_LDOS3	2.8	360	1. Camera AF 2. Touch Panel
SLDO1	VMIPI	VSYS_LDOS4 and VS1_SLDO3	1.8	300	1. RF AFE/MIPI 2. Efuse
DLDO	VIO28	VSYS_LDOS3	2.8	400	1. Sensor 2. 2.8 IO
DLDO	VMC	VSYS_LDOS2	3	800	Memory card for eMMC and UFS
DLDO	VMCH	VSYS_LDOS2	3	800	Memory card for eMMC and UFS
DLDO	VEMC	VSYS_LDOS3	3	800	Storage for eMMC and UFS
SLDO1	VUFS18	VSYS_LDOS4 and VS1_SLDO1	1.8	1000	Storage for eMMC and UFS
ALDO	VUSB33	VSYS_LDOS1	3.07	120	USB power and audio
ALDO	VBIF28	VSYS_LDOS1	2.8	20	Battery interface
SLDO1	VIO18	VSYS_LDOS4 and VS1_SLDO2	1.8	1000	1.8V IO
DLDO	VRTC	VSYSSNS or BATSNS	2.8	2	RTC
DLDO	DVDD18_DIG	VSYSSNS or BATSNS	1.8	10	PMIC internal digital power
DLDO	VGP	VSYS_LDOS2	1.89	200	General purpose
DLDO	VGP2	VSYS_LDOS1	2.8	200	General purpose

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3.2.4 Charger-In Detection

The charger-in detector senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the power-on process will be activated when system is off. This detector resists higher input voltages than other parts of PMIC.

3.2.4.1 Block Descriptions

The block diagram of battery charger is illustrated below.

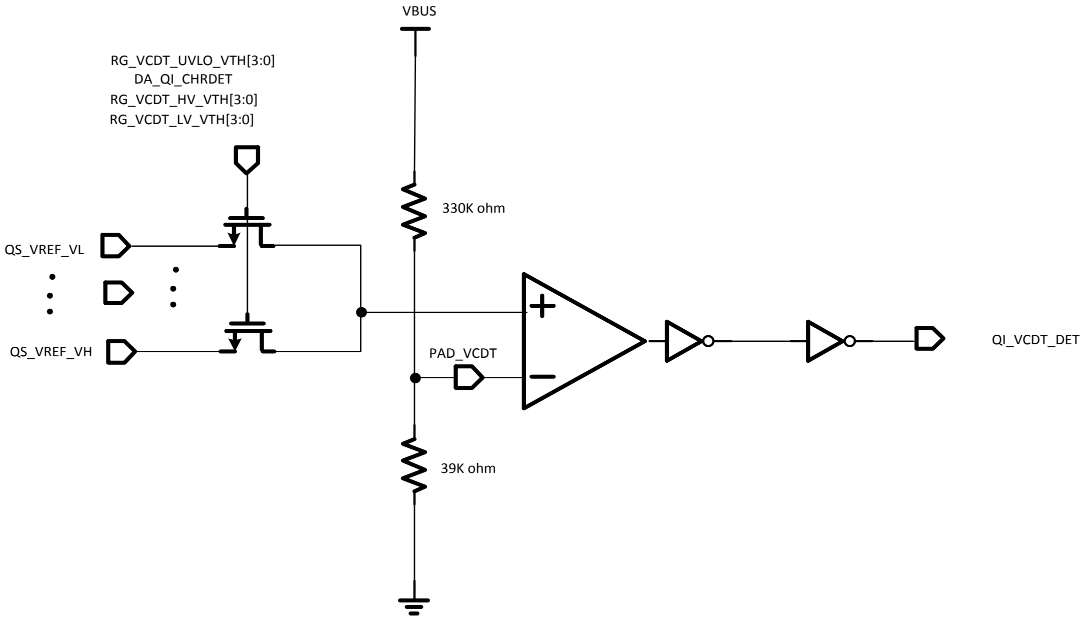

Figure 3-4. Block diagram of charger-in detection

3.2.4.1.1 Charger Detection

A charger will be judged to be invalid when the charging source level is detected too high (> 7.0V, software default setting) or too low (< 3.9V) to avoid improper charging behavior.

3.2.5 Audio CODEC and Accessory Detection

3.2.5.1 Block Descriptions

The block diagram of audio codec is illustrated below. Audio uplink path is composed of PGA and audio ADC. There are four input pairs of the uplink path to support dual-MIC, earphone-MIC, ANC-MIC, and digital-MIC. The uplink front-end to PGA can be configured as ACC or DCC type. The audio downlink is composed of stereo audio DACs, stereo headphone drivers, a mono voice driver and a

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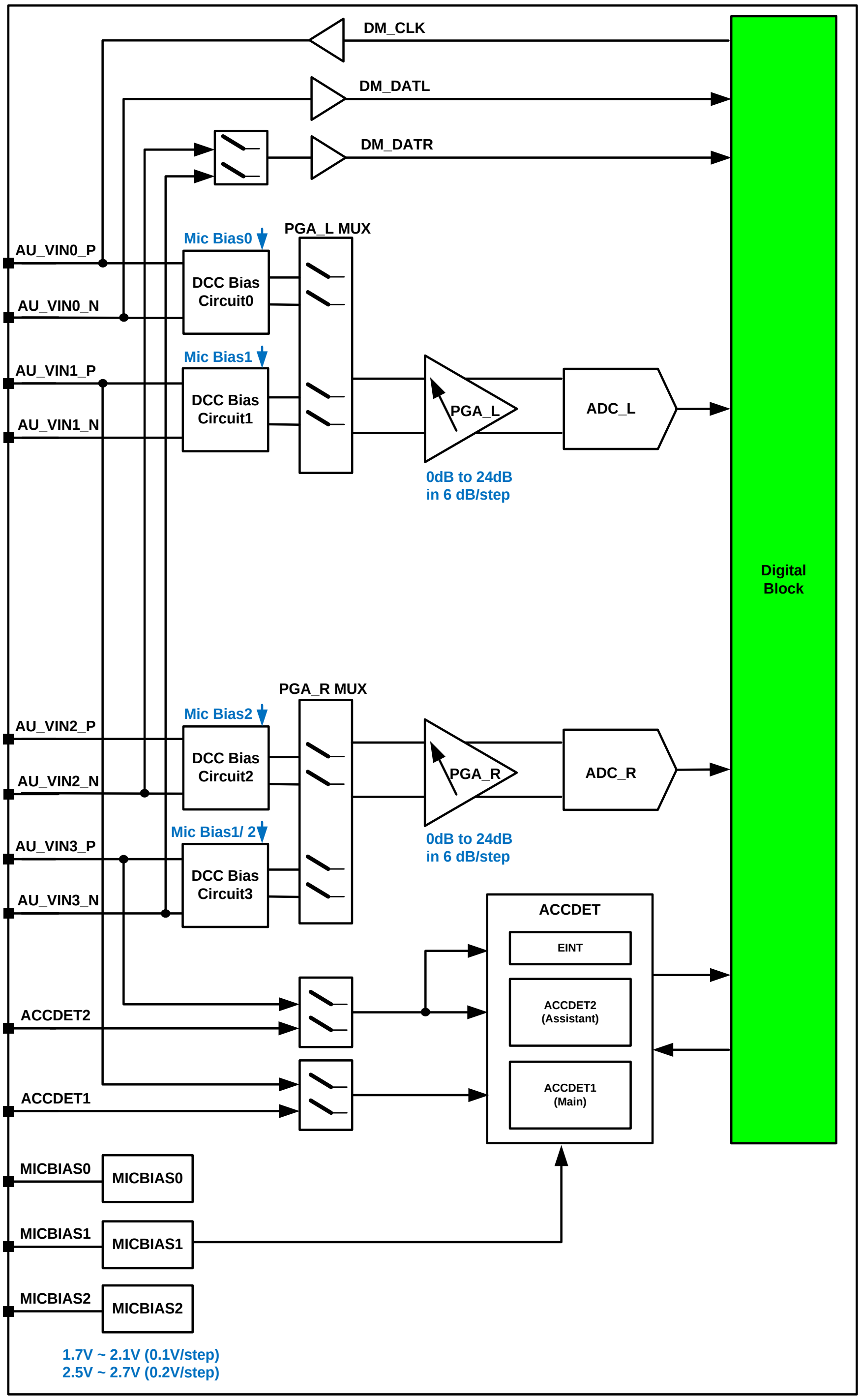
mono line-out driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The line-out driver can be used to drive external high output power loud-speaker amplifier. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.



(a) Audio/speech uplink and accessory detection

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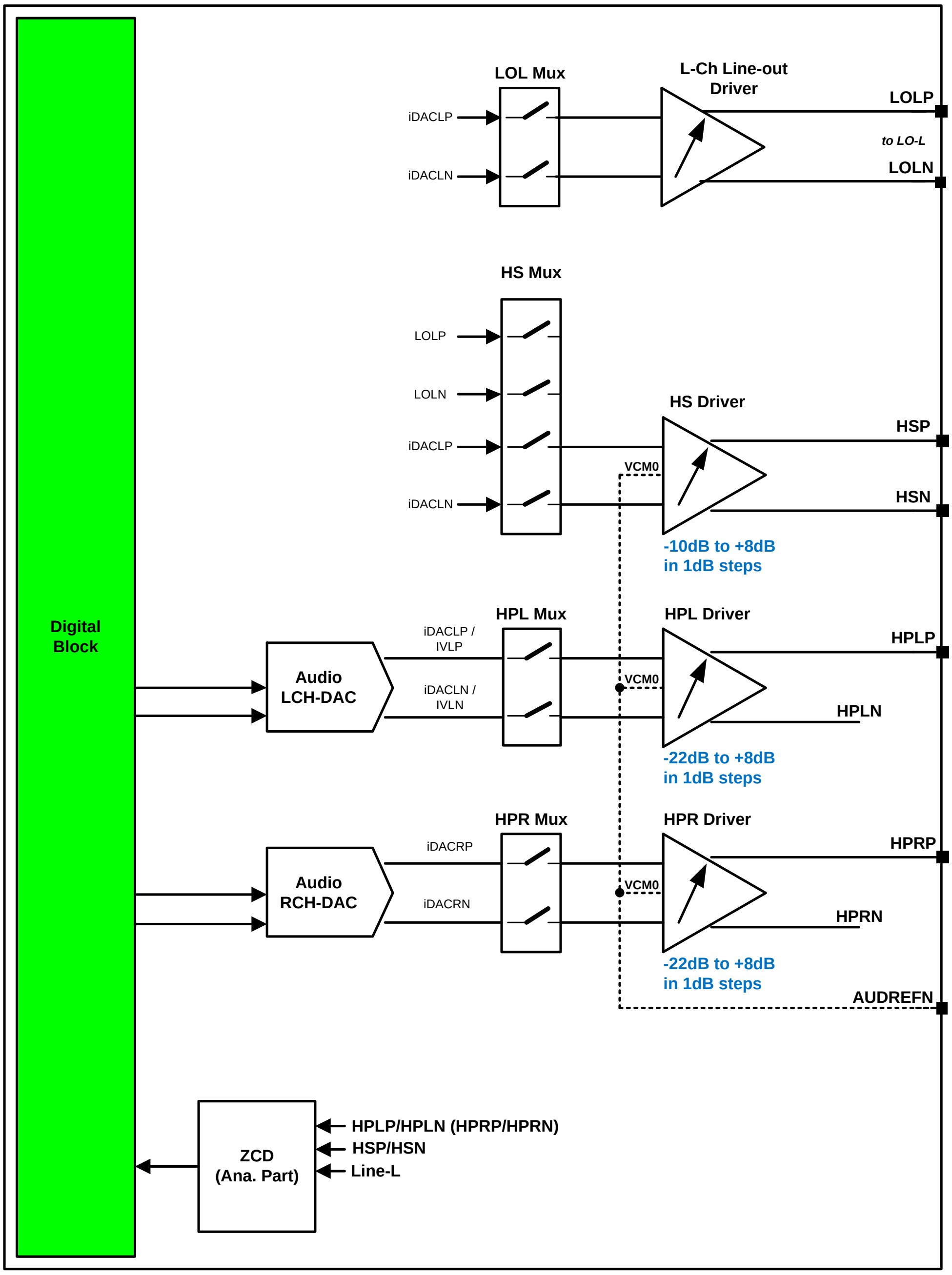

(b) Audio/speech downlink and headphone detection

Figure 3-5. Audio CODEC block diagram

3.2.6 AUXADC

3.2.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

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1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data.

Table 3-3. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATADC	2.5 ~ 5.0
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 2.7
5	ACCDET	0~1.7
7	AUXADC_VIN	0 ~ 1.8
9	HP calibration	1.5~1.7
Others	Internal use	N/A

3.2.7 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to convert the current drawn from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

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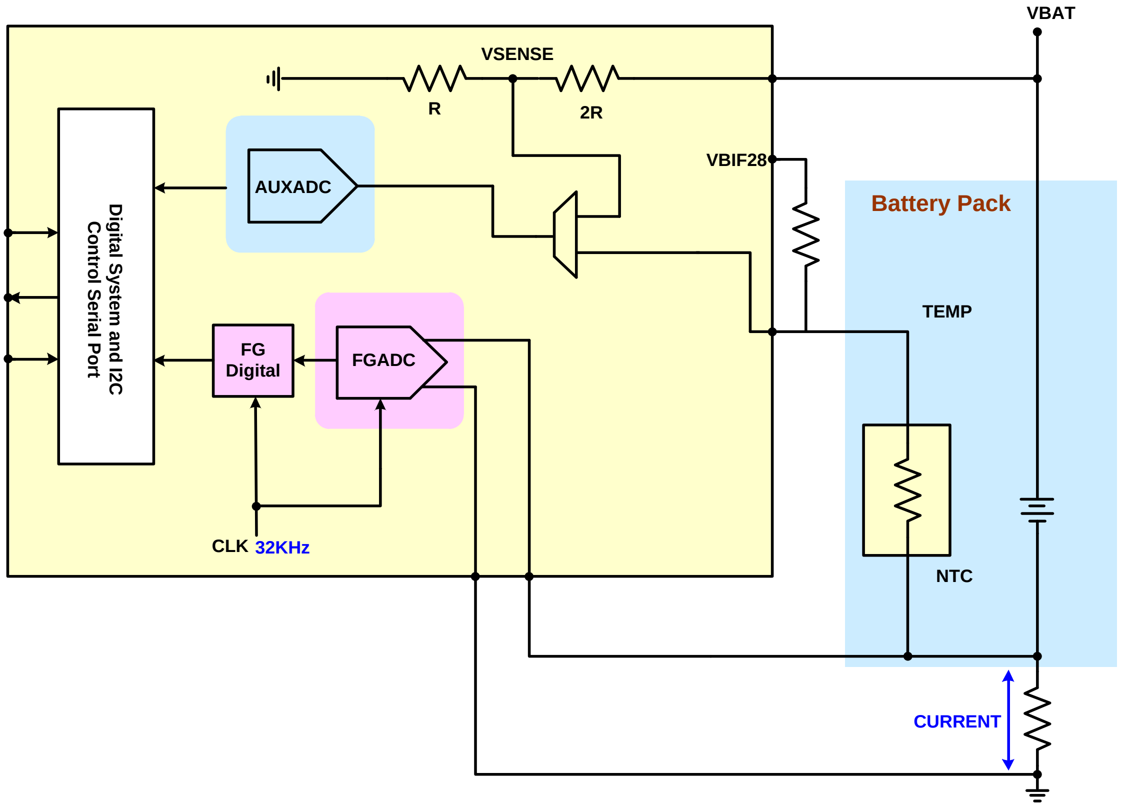

Figure 3-6. Fuel gauge block diagram and external connection

3.2.8 BIF

MIPI Battery Interface (BIF) is the first comprehensive battery communication interface standard for mobile devices. BIF module serves as a BIF master, which follows MIPI BIF protocol. It can be used to communicate with the battery package which has the BIF slave devices to monitor the battery status. Each transaction is started from a master and the slaves are the passive side.

Features:

- One wire communication
- Supports smart battery
- Single master, multi Slave
- Receives at most 10 data packets in one transaction
- Sends at most 15 data packets in one transaction

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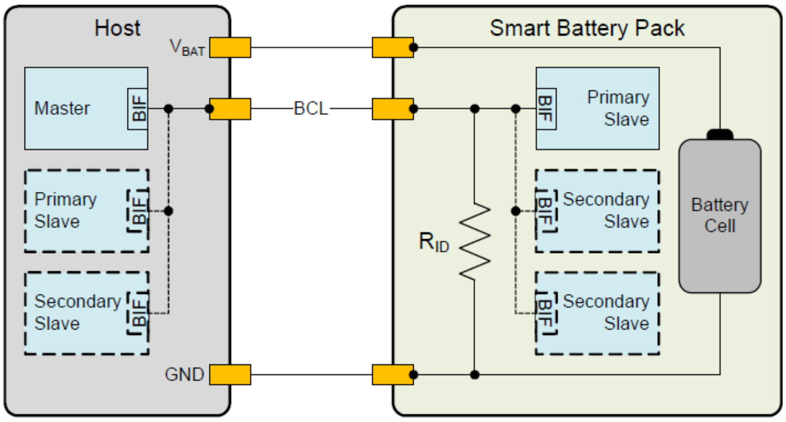

Figure 3-7. BIF application diagram

3.2.9 Real-Time Clock

The real-time clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6355, RTC module also supports function without 32kHz crystal. It can be configured by hardware option. The two configurations are shown below. When crystal is absent, RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

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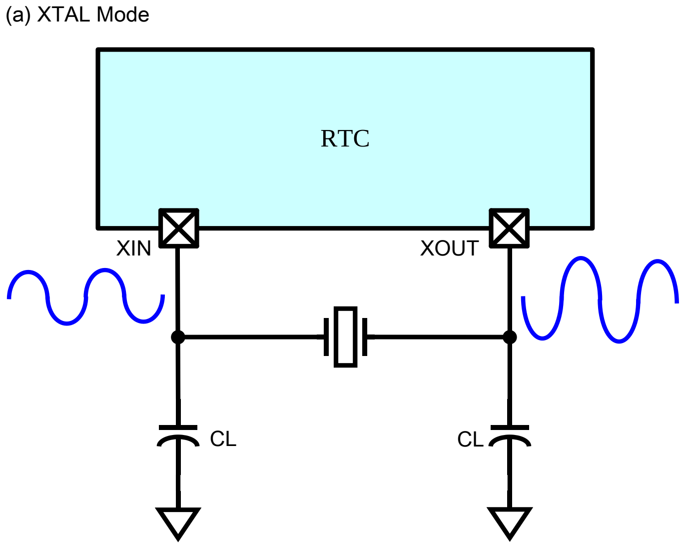

Figure 3-8. RTC configuration methods for XTAL

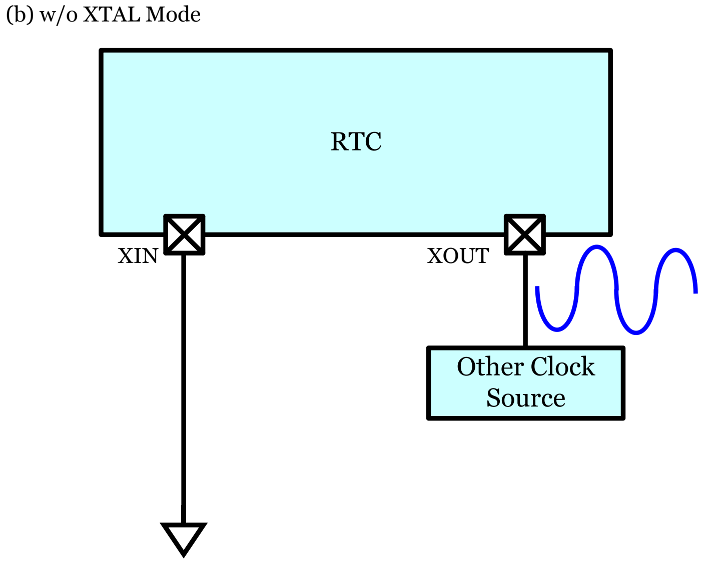

Figure 3-9. RTC configuration methods for w/o XTAL mode

3.2.9.1 32kHz Crystal Oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

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Table 3-4. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.1	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	20		80	%
I	Current consumption		5		µA
T	Operating temperature	-20		80	°C

The minimum VRTC value means if the crystal oscillator starts up successfully, then the minimum VRTC for the clock to still be alive is 1.1V.

Since the crystal parameters determine the oscillation allowance, below are a few recommendations for the crystal parameters to be used well with XOSC32 in MT6355.

Table 3-5. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level	0.5			uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	KΩ
Co	Static capacitance		0.9	2	pF
CL[1]	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is greater than 3 times. If CL is selected larger, the frequency accuracy will be decreased, and the –R will degrade too.

3.2.10 XO

3.2.10.1 Reference Clock Specification

MT6355 PMIC integrates a 26MHz XTAL oscillator (XO) and supports 32kHz RTC-removal low power mode. There are two High Performance (XO_WCN, XO_CEL), and four Low Power (XO_SOC, XO_NFC, XO_AUD, XO_EXT) external clock buffers for the whole system.

The external component, Temperature Sensing Crystal (TSX) pin#1 and pin#3 are connected to XTAL1 and XTAL2, and the other two pins are connected to AUXADC.

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3.2.10.2 Reference Output Buffer(s) Specification

There are six 26MHz clock output buffers driving out from the chip. They can be used as clock source for other chips and applications. Two High Performance (HP) external buffers output 0~1.8V squarer wave, and the other Low Noise (LN) Low Power (LP) external buffers output 0~1.1V squarer wave. Note that all their DC common mode voltage is not zero, so DC block capacitor is required if it is AC coupled and specific common mode voltage.

The current of all buffers can be optimized for different PCB Cloading. Typical current listed is limited for < 20pF Cloading.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty cycle		40		60	%
Rise/Fall time	10% to 90% of signal swing @ Cload=20pF			5	ns
HP buffer output	Square wave	1.6	1.8	2.0	Vp-p
HP SSB phase noise	1Hz offset [20pF load]			-50	dBc/Hz
	5Hz offset [20pF load]			-73	dBc/Hz
	10Hz offset [20pF load]			-80	dBc/Hz
	100Hz offset [20pF load]			-106	dBc/Hz
	1kHz offset [20pF load]			-134	dBc/Hz
	10kHz offset [20pF load]			-144	dBc/Hz
	100KHz offset [20pF load]			-152	dBc/Hz
HP current consumption	Zload = 20pF (each buffer)		2.0		mA
LP buffer output	Square wave	0.8	1.1	1.3	Vp-p
LP SSB phase noise	100Hz offset [20pF load]			-85	dBc/Hz
	1kHz offset [20pF load]			-110	dBc/Hz
	10kHz offset [20pF load]			-130	dBc/Hz
	100kHz offset [20pF load]			-130	dBc/Hz
LP current consumption	Zload = 20pF (each buffer)		1.0		mA

3.2.10.3 32kHz RTC Removal Mode

In low power mode a 32kHz clock is produced by a fractional-N divider (1st order Sigma Delta Modulated) to replace the traditional 32kHz XTAL. The capacitance is minimized for significant current reduced.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Frequency	Averaged value		32768		Hz
XO LPM current consumption (VXO22)	Low power mode With all capacitors switched off and auto-amplitude calibration on		50		µA

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Parameter	Conditions	Min.	Nom.	Max.	Unit
Duty cycle				70	%
Settling time				5	ms
Frequency variation	After system calibration			±2	ppm
	Over temperature -20°C to 75°C			15	ppm
	Uncalibrated – total variation			200	ppm

3.2.11 Interrupt and Watchdog

3.2.11.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - HOMEKEY: Interrupt is issued when HOMEKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the HOMEKEY _DEB status to see if it is pressed or released.
2. Thermal interrupt
   PMIC issues THR_H interrupt for the software high power latch if PMIC die temperature is over thermal regulation high threshold (e.g. 125°c) and issues THR_L for software latch release if PMIC die temperature goes from thermal regulation high threshold (e.g. 125°c) back to under thermal regulation low threshold (e.g. 110°c). The thermal regulation high/low threshold is adjustable.
3. Charger related interrupt
4. Battery voltage/current H/L interrupt
   There are two groups of VBAT detection interrupts.
   1) VBAT detected by AUXADC
      If VBAT is higher than the threshold specified by a register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.
   2) VBAT detected by fuel gauge
      If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.
5. Fuel-Gauge
6. Buck OC interrupt
   There are 8 bucks and each has its individual interrupt which uses PWM detection method.
7. Buck PREOC interrupt
   There is one buck preoc interrupt for VCORE.
8. LDO OC interrupt

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PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.

9. RTC interrupt
10. Novel Adaptive Fuel Gauge (NAFG) delta-V accumulation interrupt
    If the accumulation of NAFG delta-voltage is larger than the programmable threshold, this interrupt will be issued.

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Table 3-6. MT6355 interrupts

Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
STRUP	PWRKEY	RG_INT_EN_PWRKEY	0x0800 bit0	RG_INT_STATUS_PWRKEY	0x0854 bit00	edge(rising & falling)	1	32ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY	RG_INT_EN_HOMEKEY	0x0800 bit1	RG_INT_STATUS_HOMEKEY	0x0854 bit01	edge(rising & falling)	0	32ms (in STRUP)	Write 1 Clear
STRUP	PWRKEY_R	RG_INT_EN_PWRKEY_R	0x0800 bit2	RG_INT_STATUS_PWRKEY_R	0x0854 bit02	edge(rising)	1	32ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY_R	RG_INT_EN_HOMEKEY_R	0x0800 bit3	RG_INT_STATUS_HOMEKEY_R	0x0854 bit03	edge(rising)	0	32ms (in STRUP)	Write 1 Clear
STRUP	NI_LBAT_INT	RG_INT_EN_NI_LBAT_INT	0x0800 bit4	RG_INT_STATUS_NI_LBAT_INT	0x0854 bit04	edge(rising)	0	N	Write 1 Clear
STRUP	CHRDET	RG_INT_EN_CHRDET	0x0800 bit5	RG_INT_STATUS_CHRDET	0x0854 bit05	level (high & low)	1	50ms (in STRUP)	Write 1 Clear
STRUP	CHRDET_EDGE	RG_INT_EN_CHRDET_EDGE	0x0800 bit6	RG_INT_STATUS_CHRDET_EDGE	0x0854 bit06	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
BTAON	BATON_LV	RG_INT_EN_BATON_LV	0x0800 bit7	RG_INT_STATUS_BATON_LV	0x0854 bit07	level (high active)	0	N	Write 1 Clear
BTAON	BATON_HV	RG_INT_EN_BATON_HV	0x0800 bit8	RG_INT_STATUS_BATON_HV	0x0854 bit08	level (high active)	0	N	Write 1 Clear
BTAON	BATON_BAT_IN	RG_INT_EN_BATON_BAT_IN	0x0800 bit9	RG_INT_STATUS_BATON_BAT_IN	0x0854 bit09	edge(rising)	1	V(in BATON)	Write 1 Clear
BTAON	BATON_BAT_OUT	RG_INT_EN_BATON_BAT_OUT	0x0800 bit10	RG_INT_STATUS_BATON_BAT_OUT	0x0854 bit10	edge(falling)	1	V(in BATON)	Write 1 Clear
RTC	RTC	RG_INT_EN_RTC	0x0800 bit11	RG_INT_STATUS_RTC	0x0854 bit11	level (low active)	0	N	Write 1 Clear
RTC	RTC_NSEC	RG_INT_EN_RTC_NSEC	0x0800 bit12	RG_INT_STATUS_RTC_NSEC	0x0854 bit12	level (low active)	0	N	Write 1 Clear
BIF	BIF	RG_INT_EN_BIF	0x0800 bit13	RG_INT_STATUS_BIF	0x0854 bit13	level (high active)	0	N	Write 1 Clear
CHRDET	VCDT_HV_DET	RG_INT_EN_VCDT_HV_DET	0x0800 bit14	RG_INT_STATUS_VCDT_HV_DET	0x0854 bit14	level (high active)	0	N	Write 1 Clear
AUXADC	THR_H	RG_INT_EN_THR_H	0x0806 bit0	RG_INT_STATUS_THR_H	0x0856 bit00	edge(rising)	0	V (in AUXADC)	Write 1 Clear
AUXADC	THR_L	RG_INT_EN_THR_L	0x0806 bit1	RG_INT_STATUS_THR_L	0x0856 bit01	edge(rising)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_H	RG_INT_EN_BAT_H	0x0806 bit2	RG_INT_STATUS_BAT_H	0x0856 bit02	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_L	RG_INT_EN_BAT_L	0x0806 bit3	RG_INT_STATUS_BAT_L	0x0856 bit03	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT2_H	RG_INT_EN_BAT2_H	0x0806 bit4	RG_INT_STATUS_BAT2_H	0x0856 bit04	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT2_L	RG_INT_EN_BAT2_L	0x0806 bit5	RG_INT_STATUS_BAT2_L	0x0856 bit05	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_TEMP_H	RG_INT_EN_BAT_TEMP_H	0x0806 bit6	RG_INT_STATUS_BAT_TEMP_H	0x0856 bit06	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_TEMP_L	RG_INT_EN_BAT_TEMP_L	0x0806 bit7	RG_INT_STATUS_BAT_TEMP_L	0x0856 bit07	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	AUXADC_IMP	RG_INT_EN_AUXADC_IMP	0x0806 bit8	RG_INT_STATUS_AUXADC_IMP	0x0856 bit08	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	NAG_C_DLTV	RG_INT_EN_NAG_C_DLTV	0x0806 bit9	RG_INT_STATUS_NAG_C_DLTV	0x0856 bit09	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_HOT	RG_INT_EN_JEITA_HOT	0x0806 bit10	RG_INT_STATUS_JEITA_HOT	0x0856 bit10	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_WARM	RG_INT_EN_JEITA_WARM	0x0806 bit11	RG_INT_STATUS_JEITA_WARM	0x0856 bit11	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_COOL	RG_INT_EN_JEITA_COOL	0x0806 bit12	RG_INT_STATUS_JEITA_COOL	0x0856 bit12	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	JEITA_COLD	RG_INT_EN_JEITA_COLD	0x0806 bit13	RG_INT_STATUS_JEITA_COLD	0x0856 bit13	level (high active)	0	V (in AUXADC)	Write 1 Clear
Regulator	VPROC11_OC	RG_INT_EN_VPROC11_OC	0x080C bit0	RG_INT_STATUS_VPROC11_OC	0x0858 bit00	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VPROC12_OC	RG_INT_EN_VPROC12_OC	0x080C bit1	RG_INT_STATUS_VPROC12_OC	0x0858 bit01	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VCORE_OC	RG_INT_EN_VCORE_OC	0x080C bit2	RG_INT_STATUS_VCORE_OC	0x0858 bit02	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear

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Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
Regulator	VGPU_OC	RG_INT_EN_VGPU_OC	0x080C bit3	RG_INT_STATUS_VGPU_OC	0x0858 bit03	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VDRAM1_OC	RG_INT_EN_VDRAM1_OC	0x080C bit4	RG_INT_STATUS_VDRAM1_OC	0x0858 bit04	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VDRAM2_OC	RG_INT_EN_VDRAM2_OC	0x080C bit5	RG_INT_STATUS_VDRAM2_OC	0x0858 bit05	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VMODEM_OC	RG_INT_EN_VMODEM_OC	0x080C bit6	RG_INT_STATUS_VMODEM_OC	0x0858 bit06	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VS1_OC	RG_INT_EN_VS1_OC	0x080C bit7	RG_INT_STATUS_VS1_OC	0x0858 bit07	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VS2_OC	RG_INT_EN_VS2_OC	0x080C bit8	RG_INT_STATUS_VS2_OC	0x0858 bit08	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VPA_OC	RG_INT_EN_VPA_OC	0x080C bit9	RG_INT_STATUS_VPA_OC	0x0858 bit09	level (high active)	0	PMW deb (in BUCK)	Write 1 Clear
Regulator	VCORE_PREOC	RG_INT_EN_VCORE_PREOC	0x080C bit10	RG_INT_STATUS_VCORE_PREOC	0x0858 bit10	level (high active)	0	5us(in INCTRL)	Write 1 Clear
LDO	VA10_OC	RG_INT_EN_VA10_OC	0x080C bit11	RG_INT_STATUS_VA10_OC	0x0858 bit11	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VA12_OC	RG_INT_EN_VA12_OC	0x080C bit12	RG_INT_STATUS_VA12_OC	0x0858 bit12	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VA18_OC	RG_INT_EN_VA18_OC	0x080C bit13	RG_INT_STATUS_VA18_OC	0x0858 bit13	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VBIF28_OC	RG_INT_EN_VBIF28_OC	0x080C bit14	RG_INT_STATUS_VBIF28_OC	0x0858 bit14	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCAMA1_OC	RG_INT_EN_VCAMA1_OC	0x080C bit15	RG_INT_STATUS_VCAMA1_OC	0x0858 bit15	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCAMA2_OC	RG_INT_EN_VCAMA2_OC	0x0812 bit0	RG_INT_STATUS_VCAMA2_OC	0x085A bit00	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VXO18_OC	RG_INT_EN_VXO18_OC	0x0812 bit1	RG_INT_STATUS_VXO18_OC	0x085A bit01	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCAMD1_OC	RG_INT_EN_VCAMD1_OC	0x0812 bit2	RG_INT_STATUS_VCAMD1_OC	0x085A bit02	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCAMD2_OC	RG_INT_EN_VCAMD2_OC	0x0812 bit3	RG_INT_STATUS_VCAMD2_OC	0x085A bit03	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCAMIO_OC	RG_INT_EN_VCAMIO_OC	0x0812 bit4	RG_INT_STATUS_VCAMIO_OC	0x085A bit04	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCN18_OC	RG_INT_EN_VCN18_OC	0x0812 bit5	RG_INT_STATUS_VCN18_OC	0x085A bit05	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCN28_OC	RG_INT_EN_VCN28_OC	0x0812 bit6	RG_INT_STATUS_VCN28_OC	0x085A bit06	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VCN33_OC	RG_INT_EN_VCN33_OC	0x0812 bit7	RG_INT_STATUS_VCN33_OC	0x085A bit07	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VTCXO24_OC	RG_INT_EN_VTCXO24_OC	0x0812 bit8	RG_INT_STATUS_VTCXO24_OC	0x085A bit08	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VEMC_OC	RG_INT_EN_VEMC_OC	0x0812 bit9	RG_INT_STATUS_VEMC_OC	0x085A bit09	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VFE28_OC	RG_INT_EN_VFE28_OC	0x0812 bit10	RG_INT_STATUS_VFE28_OC	0x085A bit10	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VGP_OC	RG_INT_EN_VGP_OC	0x0812 bit11	RG_INT_STATUS_VGP_OC	0x085A bit11	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VLDO28_OC	RG_INT_EN_VLDO28_OC	0x0812 bit12	RG_INT_STATUS_VLDO28_OC	0x085A bit12	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VIO18_OC	RG_INT_EN_VIO18_OC	0x0812 bit13	RG_INT_STATUS_VIO18_OC	0x085A bit13	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VIO28_OC	RG_INT_EN_VIO28_OC	0x0812 bit14	RG_INT_STATUS_VIO28_OC	0x085A bit14	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VMC_OC	RG_INT_EN_VMC_OC	0x0812 bit15	RG_INT_STATUS_VMC_OC	0x085A bit15	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VMCH_OC	RG_INT_EN_VMCH_OC	0x0818 bit0	RG_INT_STATUS_VMCH_OC	0x085C bit00	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VMIPI_OC	RG_INT_EN_VMIPI_OC	0x0818 bit1	RG_INT_STATUS_VMIPI_OC	0x085C bit01	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VRF12_OC	RG_INT_EN_VRF12_OC	0x0818 bit2	RG_INT_STATUS_VRF12_OC	0x085C bit02	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VRF18_1_OC	RG_INT_EN_VRF18_1_OC	0x0818 bit3	RG_INT_STATUS_VRF18_1_OC	0x085C bit03	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VRF18_2_OC	RG_INT_EN_VRF18_2_OC	0x0818 bit4	RG_INT_STATUS_VRF18_2_OC	0x085C bit04	level (high active)	0	implement in LDO	Write 1 Clear

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Module name	Interrupt name	Enable	Enable ADR	Status	Status ADR	Level/Edge	Default EN	De-bounce time	Status clear condition
LDO	VSIM1_OC	RG_INT_EN_VSIM1_OC	0x0818 bit5	RG_INT_STATUS_VSIM1_OC	0x085C bit05	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VSIM2_OC	RG_INT_EN_VSIM2_OC	0x0818 bit6	RG_INT_STATUS_VSIM2_OC	0x085C bit06	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VGP2_OC	RG_INT_EN_VGP2_OC	0x0818 bit7	RG_INT_STATUS_VGP2_OC	0x085C bit07	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VSRAM_CORE_OC	RG_INT_EN_VSRAM_CORE_OC	0x0818 bit8	RG_INT_STATUS_VSRAM_CORE_OC	0x085C bit08	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VSRAM_PROC_OC	RG_INT_EN_VSRAM_PROC_OC	0x0818 bit9	RG_INT_STATUS_VSRAM_PROC_OC	0x085C bit09	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VSRAM_GPU_OC	RG_INT_EN_VSRAM_GPU_OC	0x0818 bit10	RG_INT_STATUS_VSRAM_GPU_OC	0x085C bit10	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VSRAM_MD_OC	RG_INT_EN_VSRAM_MD_OC	0x0818 bit11	RG_INT_STATUS_VSRAM_MD_OC	0x085C bit11	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VUFS18_OC	RG_INT_EN_VUFS18_OC	0x0818 bit12	RG_INT_STATUS_VUFS18_OC	0x085C bit12	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VUSB33_OC	RG_INT_EN_VUSB33_OC	0x0818 bit13	RG_INT_STATUS_VUSB33_OC	0x085C bit13	level (high active)	0	implement in LDO	Write 1 Clear
LDO	VXO22_OC	RG_INT_EN_VXO22_OC	0x0818 bit14	RG_INT_STATUS_VXO22_OC	0x085C bit14	level (high active)	0	implement in LDO	Write 1 Clear
FGADC	FG_BAT0_H	RG_INT_EN_FG_BAT0_H	0x081E bit0	RG_INT_STATUS_FG_BAT0_H	0x085E bit00	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT0_L	RG_INT_EN_FG_BAT0_L	0x081E bit1	RG_INT_STATUS_FG_BAT0_L	0x085E bit01	edge(rising)	0	N	Write 1 Clear
FGADC	FG_CUR_H	RG_INT_EN_FG_CUR_H	0x081E bit2	RG_INT_STATUS_FG_CUR_H	0x085E bit02	edge(rising)	0	N	Write 1 Clear
FGADC	FG_CUR_L	RG_INT_EN_FG_CUR_L	0x081E bit3	RG_INT_STATUS_FG_CUR_L	0x085E bit03	edge(rising)	0	N	Write 1 Clear
FGADC	FG_ZCV	RG_INT_EN_FG_ZCV	0x081E bit4	RG_INT_STATUS_FG_ZCV	0x085E bit04	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT1_H	RG_INT_EN_FG_BAT1_H	0x081E bit5	RG_INT_STATUS_FG_BAT1_H	0x085E bit05	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT1_L	RG_INT_EN_FG_BAT1_L	0x081E bit6	RG_INT_STATUS_FG_BAT1_L	0x085E bit06	edge(rising)	0	N	Write 1 Clear
FGADC	FG_N_CHARGE_L	RG_INT_EN_FG_N_CHARGE_L	0x081E bit7	RG_INT_STATUS_FG_N_CHARGE_L	0x085E bit07	edge(rising)	0	N	Write 1 Clear
FGADC	FG_IAVG_H	RG_INT_EN_FG_IAVG_H	0x081E bit8	RG_INT_STATUS_FG_IAVG_H	0x085E bit08	edge(rising)	0	N	Write 1 Clear
FGADC	FG_IAVG_L	RG_INT_EN_FG_IAVG_L	0x081E bit9	RG_INT_STATUS_FG_IAVG_L	0x085E bit09	edge(rising)	0	N	Write 1 Clear
FGADC	FG_TIME_H	RG_INT_EN_FG_TIME_H	0x081E bit10	RG_INT_STATUS_FG_TIME_H	0x085E bit10	edge(rising)	0	N	Write 1 Clear
FGADC	FG_DISCHARGE	RG_INT_EN_FG_DISCHARGE	0x081E bit11	RG_INT_STATUS_FG_DISCHARGE	0x085E bit11	edge(rising)	0	N	Write 1 Clear
FGADC	FG_CHARGE	RG_INT_EN_FG_CHARGE	0x081E bit12	RG_INT_STATUS_FG_CHARGE	0x085E bit12	edge(rising)	0	N	Write 1 Clear
Audio	AUDIO	RG_INT_EN_AUDIO	0x0824 bit0	RG_INT_STATUS_AUDIO	0x0860 bit00	level (high active)	0	No	Write 1 Clear
Audio	MAD	RG_INT_EN_MAD	0x0824 bit1	RG_INT_STATUS_MAD	0x0860 bit01	level (high active)	0	No	Write 1 Clear
EINT	EINT_RTC32K_1V8_1	RG_INT_EN_EINT_RTC32K_1V8_1	0x0824 bit2	RG_INT_STATUS_EINT_RTC32K_1V8_1	0x0860 bit02	eint	0	Y(in eint_top)	Write 1 Clear
EINT	EINT_AUD_CLK	RG_INT_EN_EINT_AUD_CLK	0x0824 bit3	RG_INT_STATUS_EINT_AUD_CLK	0x0860 bit03	eint	0	Y(in eint_top)	Write 1 Clear
EINT	EINT_AUD_DAT_MOSI	RG_INT_EN_EINT_AUD_DAT_MOSI	0x0824 bit4	RG_INT_STATUS_EINT_AUD_DAT_MOSI	0x0860 bit04	eint	0	Y(in eint_top)	Write 1 Clear
EINT	EINT_AUD_DAT_MISO	RG_INT_EN_EINT_AUD_DAT_MISO	0x0824 bit5	RG_INT_STATUS_EINT_AUD_DAT_MISO	0x0860 bit05	eint	0	Y(in eint_top)	Write 1 Clear
EINT	EINT_VOW_CLK_MISO	RG_INT_EN_EINT_VOW_CLK_MISO	0x0824 bit6	RG_INT_STATUS_EINT_VOW_CLK_MISO	0x0860 bit06	eint	0	Y(in eint_top)	Write 1 Clear
ACCDET	ACCDET	RG_INT_EN_ACCDET	0x0824 bit7	RG_INT_STATUS_ACCDET	0x0860 bit07	level (high active)	0	Y(in ACCDET)	Write 1 Clear
ACCDET	ACCDET_EINT	RG_INT_EN_ACCDET_EINT	0x0824 bit8	RG_INT_STATUS_ACCDET_EINT	0x0860 bit08	level (high active)	0	Y(in ACCDET)	Write 1 Clear
SPISLV	SPI_CMD_ALERT	RG_INT_EN_SPI_CMD_ALERT	0x0824 bit9	RG_INT_STATUS_SPI_CMD_ALERT	0x0860 bit09	level (high active)	0	N	Write 1 Clear

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3.2.11.2 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.12 SPI Interface

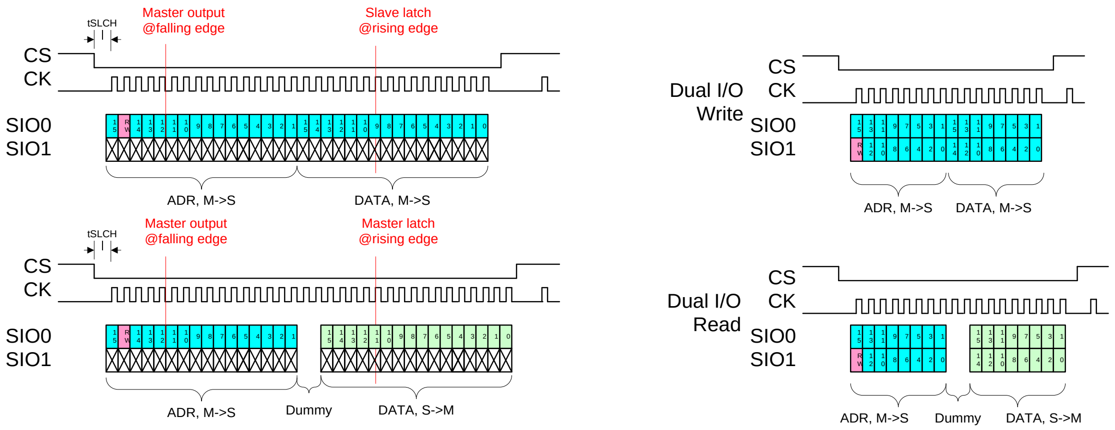
PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

3.2.12.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit 15 to bit 1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master is at the rising edge of the clock, and output data are at the falling edge of the clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



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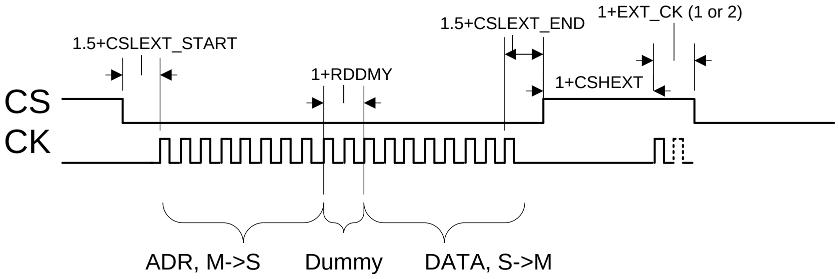
SPI parameter configuration:



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3.2.13 GPIO

3.2.13.1 GPIO List

Table 3-7. MT6355 GPIO list

Pin Name	Aux Func 0	Aux Func 1	Aux Func 2	Aux Func 3	Aux Func 4	Aux Func 5	Aux Func 6	Aux Func 7	PU/PD
PAD_HOMEKEY	GPIO0	I1: HOMEKEY	O:INT_0			I0: TEST_CK0			PU/PD
PAD_SRCLKEN_IN0	GPIO1	I1: SRCLKEN_IN0					I0: TEST_IN0	O: TEST_OUT0	PU/PD
PAD_SRCLKEN_IN1	GPIO2	I1: SRCLKEN_IN1				I0: TEST_CK1	I0: TEST_IN1	O: TEST_OUT1	PU/PD
PAD_RTC32K_1V8_0	GPIO3	O: RTC_32K1V8_0				I0: TEST_CK2	I0: TEST_IN2	O: TEST_OUT2	PU/PD
PAD_RTC32K_1V8_1	GPIO4	O: RTC_32K1V8_1	O:INT_1	I0: EINT0			I0: TEST_IN3	O: TEST_OUT3	PU/PD
PAD_SCP_VREQ_VAO	GPIO5	I0: SCP_VREQ_VAO					I0: TEST_IN4	O: TEST_OUT4	PU/PD
PAD_SPI_CLK	GPIO6	I0: SPI_CLK							PU/PD
PAD_SPI_CSN	GPIO7	I1: SPI_CSN							PU/PD
PAD_SPI_MOSI	GPIO8	B0: SPI_MOSI							PU/PD
PAD_SPI_MISO	GPIO9	B0: SPI_MISO							PU/PD
PAD_AUD_CLK	GPIO10	I0: AUD_CLK		I0: EINT1			I0: TEST_IN5	O: TEST_OUT5	PU/PD
PAD_AUD_DAT_MOSI	GPIO11	I0: AUD_DAT_MOSI		I0: EINT2			I0: TEST_IN6	O: TEST_OUT6	PU/PD
PAD_AUD_DAT_MISO	GPIO12	O: AUD_DAT_MISO		I0: EINT3	O: VOW_DAT_MISO		I0: TEST_IN7	O: TEST_OUT7	PU/PD
PAD_VOW_CLK_MISO	GPIO13	O: VOW_CLK_MISO		I0: EINT4					PU/PD

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3.2.13.2 GPIO Specification

Table 3-8. MT6355 GPIO electrical characteristics

Paramters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.65*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.35*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH (DC)	DC Output logic low voltage	0.75*VDDQ			V
VOL (DC)	DC Output logic high voltage			0.25*VDDQ	V
Leakage					
IIN	Input leakage current (any input 0V < VIN < VDDIO)	-5		5	µA
IOZ	Tri-state output leakage current	-5		5	µA
IIN	Input leakage current (VIN=3.3V/0V) for floating nwell IO	-10		10	µA
IOZ	Tri-state output leakage current for for floating nwell IO	-10		10	µA

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3.3 Register Table and Descriptions

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register Function
0202	TEST_OUT	16	TEST_OUT
020E	PGSTATUS0	16	Power Good Status 0
0210	PGSTATUS1	16	Power Good Status 1
0212	PSOCSTATUS	16	Power Source OC Status
0216	TOPSTATUS	16	TOP Status
021C	SMT_CON0	16	SMT_CON0
021E	SMT_CON1	16	SMT_CON1
044C	TOP_CLKSQ	16	TOP_CLKSQ Register
0452	TOP_CLKSQ_RTC	16	TOP_CLKSQ_RTC Register
0458	TOP_CLK_TRIM	16	TOP_CLK_TRIM Register
060E	TOP_RST_MISC	16	Reset Control Misc
0C4E	RG_SPI_CON3	16	SPI Control Register 3
0C50	RG_SPI_CON4	16	SPI Control Register 4
0C52	RG_SPI_CON5	16	SPI Control Register 5
0C54	RG_SPI_CON6	16	SPI Control Register 6
0C56	RG_SPI_CON7	16	SPI Control Register 7
0C58	RG_SPI_CON8	16	SPI Control Register 8
0E08	STRUP_CON4	16	STRUP Control Register N4
0E1A	STRUP_CON13	16	STRUP Control Register 13
0E2C	STRUP_ANA_CON1	16	STRUP_ANA Control Register 1
0E2E	PPCCTL0	16	PPC Control 0 Register
100C	BUCK_OC_CON0	16	BUCK_OC Control Register 0
101A	BUCK_VPROC11_CON0	16	BUCK VPROC11 CONTROL 0
101C	BUCK_VPROC11_CON1	16	BUCK VPROC11 CONTROL 1
101E	BUCK_VPROC11_CON2	16	BUCK VPROC11 CONTROL 2
103C	BUCK_VPROC12_CON0	16	BUCK VPROC12 CONTROL 0
103E	BUCK_VPROC12_CON1	16	BUCK VPROC12 CONTROL 1
1040	BUCK_VPROC12_CON2	16	BUCK VPROC12 CONTROL 2
105E	BUCK_VCORE_CON0	16	BUCK VCORE CONTROL 0
1060	BUCK_VCORE_CON1	16	BUCK VCORE CONTROL 1
1062	BUCK_VCORE_CON2	16	BUCK VCORE CONTROL 2
1082	BUCK_VGPU_CON0	16	BUCK VGPU CONTROL 0
1084	BUCK_VGPU_CON1	16	BUCK VGPU CONTROL 1
1086	BUCK_VGPU_CON	16	BUCK VGPU CONTROL 2

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Address	Name	Width	Register Function
	2		
10A4	BUCK_VDRAM1_CON0	16	BUCK VDRAM1 Control 0
10A6	BUCK_VDRAM1_CON1	16	BUCK VDRAM1 Control 1
10A8	BUCK_VDRAM1_CON2	16	BUCK VDRAM1 Control 2
10C6	BUCK_VDRAM2_CON0	16	BUCK VDRAM2 Control 0
10C8	BUCK_VDRAM2_CON1	16	BUCK VDRAM2 Control 1
10CA	BUCK_VDRAM2_CON2	16	BUCK VDRAM2 Control 2
10E8	BUCK_VMODEM_CON0	16	BUCK VMODEM Control 0
10EA	BUCK_VMODEM_CON1	16	BUCK VMODEM Control 1
10EC	BUCK_VMODEM_CON2	16	BUCK VMODEM Control 2
1112	BUCK_VS1_CON0	16	BUCK VS1 Control 0
113C	BUCK_VS2_CON0	16	BUCK VS2 Control 0
1166	BUCK_VPA_CON0	16	BUCK VPA Control 0
1168	BUCK_VPA_CON1	16	BUCK VPA Control 1
1204	SMPS_ANA_CON2	16	SMPS Control Register 2
1206	SMPS_ANA_CON3	16	SMPS Control Register 3
1208	SMPS_ANA_CON4	16	SMPS Control Register 4
120A	SMPS_ANA_CON5	16	SMPS Control Register 5
1212	SMPS_ANA_CON9	16	SMPS Control Register 9
1214	SMPS_ANA_CON10	16	SMPS Control Register 10
1216	SMPS_ANA_CON11	16	SMPS Control Register 11
1218	SMPS_ANA_CON12	16	SMPS Control Register 12
121A	SMPS_ANA_CON13	16	SMPS Control Register 13
121C	SMPS_ANA_CON14	16	SMPS Control Register 14
160E	LDO_VIO28_CON1	16	LDO VIO28 Control Register 1
1622	LDO_VIO18_CON1	16	LDO VIO18 Control Register 1
1636	LDO_VUFS18_CON1	16	LDO VUFS18 Control Register 1
164C	LDO_VA10_CON2	16	LDO VA10 Control Register 2
1660	LDO_VA12_CON1	16	LDO VA12 Control Register 1
1674	LDO_VA18_CON1	16	LDO VA18 Control Register 1
168A	LDO_VUSB33_CON1	16	LDO VUSB33 Control Register 1
169E	LDO_VEMC_CON1	16	LDO VEMC Control Register 1
16B2	LDO_VXO22_CON1	16	LDO VXO22 Control Register 1
16C6	LDO_VXO18_CON1	16	LDO VXO18 Control Register 1
16CC	LDO_VSIM1_CON0	16	LDO VSIM1 Control Register 0
16CE	LDO_VSIM1_OP_EN	16	LDO VSIM1 Operation Enable
16DA	LDO_VSIM1_CON1	16	LDO VSIM1 Control Register 1

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Address	Name	Width	Register Function
16E0	**LDO_VSIM2_CON0**	16	LDO VSIM2 Control Register 0
16E2	**LDO_VSIM2_OP_EN**	16	LDO VSIM2 Operation Enable
16EE	**LDO_VSIM2_CON1**	16	LDO VSIM2 Control Register 1
16F4	**LDO_VCAMD1_CON0**	16	LDO VCAMD1 Control Register 0
16F6	**LDO_VCAMD1_OP_EN**	16	LDO VCAMD1 Operation Enable
1702	**LDO_VCAMD1_CON1**	16	LDO VCAMD1 Control Register 1
1708	**LDO_VCAMD2_CON0**	16	LDO VCAMD2 Control Register 0
170A	**LDO_VCAMD2_OP_EN**	16	LDO VCAMD2 Operation Enable
1716	**LDO_VCAMD2_CON1**	16	LDO VCAMD2 Control Register 1
171C	**LDO_VCAMIO_CON0**	16	LDO VCAMIO Control Register 0
171E	**LDO_VCAMIO_OP_EN**	16	LDO VCAMIO Operation Enable
172A	**LDO_VCAMIO_CON1**	16	LDO VCAMIO Control Register 1
1730	**LDO_VMIPI_CON0**	16	LDO VMIPI Control Register 0
1732	**LDO_VMIPI_OP_EN**	16	LDO VMIPI Operation Enable
173E	**LDO_VMIPI_CON1**	16	LDO VMIPI Control Register 1
1744	**LDO_VGP_CON0**	16	LDO VGP Control Register 0
1746	**LDO_VGP_OP_EN**	16	LDO VGP Operation Enable
1752	**LDO_VGP_CON1**	16	LDO VGP Control Register 1
1758	**LDO_VCN33_CON0_BT**	16	LDO VCN33 bt Control Register 0
175A	**LDO_VCN33_OP_EN**	16	LDO VCN33 Operation Enable
1766	**LDO_VCN33_CON0_WIFI**	16	LDO VCN33 wifi Control Register 0
1768	**LDO_VCN33_CON1**	16	LDO VCN33 Control Register 1
176E	**LDO_VCN18_CON0**	16	LDO VCN18 Control Register 0
1770	**LDO_VCN18_OP_EN**	16	LDO VCN18 Operation Enable
177C	**LDO_VCN18_CON1**	16	LDO VCN18 Control Register 1
1782	**LDO_VCN28_CON0**	16	LDO VCN28 Control Register 0
1784	**LDO_VCN28_OP_EN**	16	LDO VCN28 Operation Enable
1790	**LDO_VCN28_CON1**	16	LDO VCN28 Control Register 1
1796	**LDO_VBIF28_CON0**	16	LDO VBIF28 Control Register 0
1798	**LDO_VBIF28_OP_EN**	16	LDO VBIF28 Operation Enable
17A4	**LDO_VBIF28_CON1**	16	LDO VBIF28 Control Register 1
17AA	**LDO_VTCXO24_CO**	16	LDO VTCXO24 Control Register 0

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Address	Name	Width	Register Function
	N0		
17AC	LDO_VTCXO24_OP_EN	16	LDO VTCXO24 Operation Enable
17B8	LDO_VTCXO24_CON1	16	LDO VTCXO24 Control Register 1
17BE	LDO_VLDO28_CON0_AF	16	LDO VLDO28 AF Control Register 0
17C0	LDO_VLDO28_OP_EN	16	LDO VLDO28 Operation Enable
17CE	LDO_VLDO28_CON1	16	LDO VLDO28 Control Register 1
17D4	LDO_VGP2_CON0	16	LDO VGP2 Control Register 0
17D6	LDO_VGP2_OP_EN	16	LDO VGP2 Operation Enable
17E2	LDO_VGP2_CON1	16	LDO VGP2 Control Register 1
1800	LDO_VFE28_CON0	16	LDO VFE28 Control Register 0
1802	LDO_VFE28_OP_EN	16	LDO VFE28 OPERATION ENABLE
180E	LDO_VFE28_CON1	16	LDO VFE28 Control Register 1
1814	LDO_VMCH_CON0	16	LDO VMCH Control Register 0
1816	LDO_VMCH_OP_EN	16	LDO VMCH OPERATION ENABLE
1822	LDO_VMCH_CON1	16	LDO VMCH Control Register 1
1828	LDO_VMC_CON0	16	LDO VMC Control Register 0
182A	LDO_VMC_OP_EN	16	LDO VMC OPERATION ENABLE
1836	LDO_VMC_CON1	16	LDO VMC Control Register 1
183C	LDO_VRF18_1_CON0	16	LDO VRF18_1 Control Register 0
183E	LDO_VRF18_1_OP_EN	16	LDO VRF18_1 OPERATION ENABLE
184A	LDO_VRF18_1_CON1	16	LDO VRF18_1 Control Register 1
1850	LDO_VRF18_2_CON0	16	LDO VRF18_2 Control Register 0
1852	LDO_VRF18_2_OP_EN	16	LDO VRF18_2 OPERATION ENABLE
185E	LDO_VRF18_2_CON1	16	LDO VRF18_2 Control Register 1
1864	LDO_VRF12_CON0	16	LDO VRF12 Control Register 0
1866	LDO_VRF12_OP_EN	16	LDO VRF12 OPERATION ENABLE
1872	LDO_VRF12_CON1	16	LDO VRF12 Control Register 1
1878	LDO_VCAMA1_CON0	16	LDO VCAMA1 Control Register 0
187A	LDO_VCAMA1_OP_EN	16	LDO VCAMA1 OPERATION ENABLE
1886	LDO_VCAMA1_CON1	16	LDO VCAMA1 Control Register 1
188C	LDO_VCAMA2_CON0	16	LDO VCAMA2 Control Register 0
188E	LDO_VCAMA2_OP_EN	16	LDO VCAMA2 OPERATION ENABLE

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Address	Name	Width	Register Function
189A	LDO_VCAMA2_CON1	16	LDO VCAMA2 Control Register 1
18A2	VRTC_CON0	16	VRTC Control Register 0
18BE	LDO_VSRAM_PROC_CON3	16	LDO VSRAM_PROC Control Register 3
18C6	LDO_VSRAM_PROC_DBG1	16	LDO VSRAM_PROC DEBUG 1
18DE	LDO_VSRAM_CORE_CON3	16	LDO VSRAM_CORE Control Register 3
18E6	LDO_VSRAM_CORE_DBG1	16	LDO VSRAM_CORE DEBUG 1
18FE	LDO_VSRAM_GPU_CON3	16	LDO VSRAM_GPU Control Register 3
1906	LDO_VSRAM_GPU_DBG1	16	LDO VSRAM_GPU DEBUG 1
191E	LDO_VSRAM_MD_CON3	16	LDO VSRAM_MD Control Register 3
1926	LDO_VSRAM_MD_DBG1	16	LDO VSRAM_MD DEBUG 1
1A00	ALDO_ANA_CON0	16	ALDO Control Register 0
1A04	ALDO_ANA_CON2	16	ALDO Control Register 2
1A0C	ALDO_ANA_CON6	16	ALDO Control Register 6
1A10	ALDO_ANA_CON8	16	ALDO Control Register 8
1A14	ALDO_ANA_CON10	16	ALDO Control Register 10
1A20	ALDO_ANA_CON16	16	ALDO Control Register 16
1A24	ALDO_ANA_CON18	16	ALDO Control Register 18
1A2C	DLDO_ANA_CON2	16	DLDO Control Register 2
1A30	DLDO_ANA_CON4	16	DLDO Control Register 4
1A34	DLDO_ANA_CON6	16	DLDO Control Register 6
1A3C	DLDO_ANA_CON10	16	DLDO Control Register 10
1A40	DLDO_ANA_CON12	16	DLDO Control Register 12
1A48	DLDO_ANA_CON16	16	DLDO Control Register 16
1A4C	SLDO20_ANA_CON0	16	SLDO20 Control Register 0
1A50	SLDO20_ANA_CON2	16	SLDO20 Control Register 2
1A54	SLDO20_ANA_CON4	16	SLDO20 Control Register 4
1A58	SLDO20_ANA_CON6	16	SLDO20 Control Register 6
1A5C	SLDO20_ANA_CON8	16	SLDO20 Control Register 8
1A6C	SLDO14_ANA_CON0	16	SLDO14 Control Register 0
1A70	SLDO14_ANA_CON2	16	SLDO14 Control Register 2
1A74	SLDO14_ANA_CON4	16	SLDO14 Control Register 4

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Address	Name	Width	Register Function
1C00	ACCDET_CON0	16	ACCDET Control Register 0
1C02	ACCDET_CON1	16	ACCDET Control Register 1
1C04	ACCDET_CON2	16	ACCDET control register 2
1C06	ACCDET_CON3	16	ACCDET Control Register 3
1C08	ACCDET_CON4	16	ACCDET Control Register 4
1C0A	ACCDET_CON5	16	ACCDET Control Register 5
1C0C	ACCDET_CON6	16	ACCDET Control Register 6
1C0E	ACCDET_CON7	16	ACCDET Control Register 7
1C10	ACCDET_CON8	16	ACCDET Control Register 8
1C12	ACCDET_CON9	16	ACCDET Control Register 9
1C14	ACCDET_CON10	16	ACCDET Control Register 10
1C18	ACCDET_CON12	16	ACCDET Control Register 12
1C1C	ACCDET_CON14	16	ACCDET Control Register 14
1C1E	ACCDET_CON15	16	ACCDET Control Register 15
1C20	ACCDET_CON16	16	ACCDET Control Register 16
1C24	ACCDET_CON18	16	ACCDET Control Register 18
1E18	OTP_CON12	16	OTP Control Register 12
1E1A	OTP_CON13	16	OTP Control Register 13
1E1C	OTP_CON14	16	OTP Control Register 14
1E1E	OTP_DOUT_0_15	16	OTP dout 0 15
1E20	OTP_DOUT_16_31	16	OTP dout 16 31
1E22	OTP_DOUT_32_47	16	OTP dout 32 47
1E24	OTP_DOUT_48_63	16	OTP dout 48 63
1E26	OTP_DOUT_64_79	16	OTP dout 64 79
1E28	OTP_DOUT_80_95	16	OTP dout 80 95
1E2A	OTP_DOUT_96_111	16	OTP dout 96 111
1E2C	OTP_DOUT_112_127	16	OTP dout 112 127
1E2E	OTP_DOUT_128_143	16	OTP dout 128 143
1E30	OTP_DOUT_144_159	16	OTP dout 144 159
1E32	OTP_DOUT_160_175	16	OTP dout 160 175
1E34	OTP_DOUT_176_191	16	OTP dout 176 191
1E36	OTP_DOUT_192_207	16	OTP dout 192 207
1E38	OTP_DOUT_208_223	16	OTP dout 208 223
1E3A	OTP_DOUT_224_239	16	OTP dout 224 239
1E3C	OTP_DOUT_240_255	16	OTP dout 240 255
1E3E	OTP_DOUT_256_271	16	OTP dout 256 271
1E40	OTP_DOUT_272_287	16	OTP dout 272 287

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Address	Name	Width	Register Function
1E42	OTP_DOUT_288_303	16	OTP dout 288 303
1E44	OTP_DOUT_304_319	16	OTP dout 304 319
1E46	OTP_DOUT_320_335	16	OTP dout 320 335
1E48	OTP_DOUT_336_351	16	OTP dout 336 351
1E4A	OTP_DOUT_352_367	16	OTP dout 352 367
1E4C	OTP_DOUT_368_383	16	OTP dout 368 383
1E4E	OTP_DOUT_384_399	16	OTP dout 384 399
1E50	OTP_DOUT_400_415	16	OTP dout 400 415
1E52	OTP_DOUT_416_431	16	OTP dout 416 431
1E54	OTP_DOUT_432_447	16	OTP dout 432 447
1E56	OTP_DOUT_448_463	16	OTP dout 448 463
1E58	OTP_DOUT_464_479	16	OTP dout 464 479
1E5A	OTP_DOUT_480_495	16	OTP dout 480 495
1E5C	OTP_DOUT_496_511	16	OTP dout 496 511
1E5E	OTP_DOUT_512_527	16	OTP dout 512 527
1E60	OTP_DOUT_528_543	16	OTP dout 528 543
1E62	OTP_DOUT_544_559	16	OTP dout 544 559
1E64	OTP_DOUT_560_575	16	OTP dout 560 575
1E66	OTP_DOUT_576_591	16	OTP dout 576 591
1E68	OTP_DOUT_592_607	16	OTP dout 592 607
1E6A	OTP_DOUT_608_623	16	OTP dout 608 623
1E6C	OTP_DOUT_624_639	16	OTP dout 624 639
1E6E	OTP_DOUT_640_655	16	OTP dout 640 655
1E70	OTP_DOUT_656_671	16	OTP dout 656 671
1E72	OTP_DOUT_672_687	16	OTP dout 672 687
1E74	OTP_DOUT_688_703	16	OTP dout 688 703
1E76	OTP_DOUT_704_719	16	OTP dout 704 719

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Address	Name	Width	Register Function
1E78	OTP_DOUT_720_735	16	OTP dout 720 735
1E7A	OTP_DOUT_736_751	16	OTP dout 736 751
1E7C	OTP_DOUT_752_767	16	OTP dout 752 767
1E7E	OTP_DOUT_768_783	16	OTP dout 768 783
1E80	OTP_DOUT_784_799	16	OTP dout 784 799
1E82	OTP_DOUT_800_815	16	OTP dout 800 815
1E84	OTP_DOUT_816_831	16	OTP dout 816 831
1E86	OTP_DOUT_832_847	16	OTP dout 832 847
1E88	OTP_DOUT_848_863	16	OTP dout 848 863
1E8A	OTP_DOUT_864_879	16	OTP dout 864 879
1E8C	OTP_DOUT_880_895	16	OTP dout 880 895
1E8E	OTP_DOUT_896_911	16	OTP dout 896 911
1E90	OTP_DOUT_912_927	16	OTP dout 912 927
1E92	OTP_DOUT_928_943	16	OTP dout 928 943
1E94	OTP_DOUT_944_959	16	OTP dout 944 959
1E96	OTP_DOUT_960_975	16	OTP dout 960 975
1E98	OTP_DOUT_976_991	16	OTP dout 976 991
1E9A	OTP_DOUT_992_1007	16	OTP dout 992 1007
1E9C	OTP_DOUT_1008_1023	16	OTP dout 1008 1023
1E9E	OTP_DOUT_1024_1039	16	OTP dout 1024 1039
1EA0	OTP_DOUT_1040_1055	16	OTP dout 1040 1055
1EA2	OTP_DOUT_1056_1071	16	OTP dout 1056 1071
1EA4	OTP_DOUT_1072_1087	16	OTP dout 1072 1087
1EA6	OTP_DOUT_1088_1103	16	OTP dout 1088 1103
1EA8	OTP_DOUT_1104_1119	16	OTP dout 1104 1119
1EAA	OTP_DOUT_1120_1135	16	OTP dout 1120 1135
1EAC	OTP_DOUT_1136_1151	16	OTP dout 1136 1151

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Address	Name	Width	Register Function
1EAE	**OTP_DOUT_1152_1167**	16	OTP dout 1152 1167
1EB0	**OTP_DOUT_1168_1183**	16	OTP dout 1168 1183
1EB2	**OTP_DOUT_1184_1199**	16	OTP dout 1184 1199
1EB4	**OTP_DOUT_1200_1215**	16	OTP dout 1200 1215
1EB6	**OTP_DOUT_1216_1231**	16	OTP dout 1216 1231
1EB8	**OTP_DOUT_1232_1247**	16	OTP dout 1232 1247
1EBA	**OTP_DOUT_1248_1263**	16	OTP dout 1248 1263
1EBC	**OTP_DOUT_1264_1279**	16	OTP dout 1264 1279
1EBE	**OTP_DOUT_1280_1295**	16	OTP dout 1280 1295
1EC0	**OTP_DOUT_1296_1311**	16	OTP dout 1296 1311
1EC2	**OTP_DOUT_1312_1327**	16	OTP dout 1312 1327
1EC4	**OTP_DOUT_1328_1343**	16	OTP dout 1328 1343
1EC6	**OTP_DOUT_1344_1359**	16	OTP dout 1344 1359
1EC8	**OTP_DOUT_1360_1375**	16	OTP dout 1360 1375
1ECA	**OTP_DOUT_1376_1391**	16	OTP dout 1376 1391
1ECC	**OTP_DOUT_1392_1407**	16	OTP dout 1392 1407
1ECE	**OTP_DOUT_1408_1423**	16	OTP dout 1408 1423
1ED0	**OTP_DOUT_1424_1439**	16	OTP dout 1424 1439
1ED2	**OTP_DOUT_1440_1455**	16	OTP dout 1440 1455
1ED4	**OTP_DOUT_1456_1471**	16	OTP dout 1456 1471
1ED6	**OTP_DOUT_1472_1487**	16	OTP dout 1472 1487
1ED8	**OTP_DOUT_1488_1503**	16	OTP dout 1488 1503
1EDA	**OTP_DOUT_1504_1519**	16	OTP dout 1504 1519
1EDC	**OTP_DOUT_1520_1535**	16	OTP dout 1520 1535
200C	**DCXO_CW04**	16	DCXO Code Word 4
200E	**DCXO_CW05**	16	DCXO Code Word 5
2010	**DCXO_CW06**	16	DCXO Code Word 6
2026	**DCXO_CW15**	16	DCXO Code Word 15
2028	**DCXO_CW16**	16	DCXO Code Word 16

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Address	Name	Width	Register Function
202C	DCXO_CW18	16	DCXO Code Word 18
202E	DCXO_CW19	16	DCXO Code Word 19
2200	CHR_CON0	16	Charger Control Register 0
2202	CHR_CON1	16	Charger Control Register 1
220A	CHR_CON5	16	Charger Control Register 5
220E	CHR_CON7	16	Charger Control Register 7
2210	PCHR_VREF_ANA_DA0	16	PCHR_VREF DA Register 0
2214	PCHR_VREF_ANA_CON1	16	PCHR_VREF Control Register 1
2216	PCHR_VREF_ANA_CON2	16	PCHR_VREF Control Register 2
2218	PCHR_VREF_ANA_CON3	16	PCHR_VREF Control Register 3
2400	GPIO_DIR0	16	GPIO Direction Control Register 0
2402	GPIO_DIR0_SET	16	GPIO_DIR0 Register SET
2404	GPIO_DIR0_CLR	16	GPIO_DIR0 Register CLR
2406	GPIO_PULLEN0	16	GPIO Pull-up/Pull-down Enable Register 0
2408	GPIO_PULLEN0_SET	16	GPIO_PULLEN0 Register SET
240A	GPIO_PULLEN0_CLR	16	GPIO_PULLEN0 Register CLR
240C	GPIO_PULLSEL0	16	GPIO Pull-up/Pull-down Selection Register 0
240E	GPIO_PULLSEL0_SET	16	GPIO_PULLSEL0 Register SET
2410	GPIO_PULLSEL0_CLR	16	GPIO_PULLSEL0 Register CLR
2412	GPIO_DINV0	16	GPIO Data Inversion Control Register 0
2414	GPIO_DINV0_SET	16	GPIO_DINV0 Register SET
2416	GPIO_DINV0_CLR	16	GPIO_DINV0 Register CLR
2418	GPIO_DOUT0	16	GPIO Data Output Register 0
241A	GPIO_DOUT0_SET	16	GPIO_DOUT0 Register SET
241C	GPIO_DOUT0_CLR	16	GPIO_DOUT0 Register CLR
241E	GPIO_PI0	16	GPIO Data Input Register 0
2420	GPIO_POE0	16	GPIO Data Direction Register 0
2422	GPIO_MODE0	16	GPIO Mode Control Register 0
2424	GPIO_MODE0_SET	16	GPIO_MODE0 Register SET
2426	GPIO_MODE0_CLR	16	GPIO_MODE0 Register CLR
2428	GPIO_MODE1	16	GPIO Mode Control Register 1
242A	GPIO_MODE1_SET	16	GPIO_MODE1 Register SET
242C	GPIO_MODE1_CLR	16	GPIO_MODE1 Register CLR
242E	GPIO_MODE2	16	GPIO Mode Control Register 2
2430	GPIO_MODE2_SET	16	GPIO_MODE2 Register SET
2432	GPIO_MODE2_CLR	16	GPIO_MODE2 Register CLR
2434	GPIO_RSV	16	
2E00	BIF_CON0	16	BIF Control Register 0
2E02	BIF_CON1	16	BIF Control Register 1

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Address	Name	Width	Register Function
2E04	BIF_CON2	16	BIF Control Register 2
2E06	BIF_CON3	16	BIF Control Register 3
2E08	BIF_CON4	16	BIF Control Register 4
2E0A	BIF_CON5	16	BIF Control Register 5
2E0C	BIF_CON6	16	BIF Control Register 6
2E0E	BIF_CON7	16	BIF Control Register 7
2E10	BIF_CON8	16	BIF Control Register 8
2E12	BIF_CON9	16	BIF Control Register 9
2E14	BIF_CON10	16	BIF Control Register 10
2E16	BIF_CON11	16	BIF Control Register 11
2E18	BIF_CON12	16	BIF Control Register 12
2E1A	BIF_CON13	16	BIF Control Register 13
2E1C	BIF_CON14	16	BIF Control Register 14
2E1E	BIF_CON15	16	BIF Control Register 15
2E20	BIF_CON16	16	BIF Control Register 16
2E22	BIF_CON17	16	BIF Control Register 17
2E24	BIF_CON18	16	BIF Control Register 18
2E26	BIF_CON19	16	BIF Control Register 19
2E28	BIF_CON20	16	BIF Control Register 20
2E2A	BIF_CON21	16	BIF Control Register 21
2E2C	BIF_CON22	16	BIF Control Register 22
2E2E	BIF_CON23	16	BIF Control Register 23
2E30	BIF_CON24	16	BIF Control Register 24
2E32	BIF_CON25	16	BIF Control Register 25
2E34	BIF_CON26	16	BIF Control Register 26
2E36	BIF_CON27	16	BIF Control Register 27
2E38	BIF_CON28	16	BIF Control Register 28
2E3A	BIF_CON29	16	BIF Control Register 29
2E3E	BIF_CON31	16	BIF Control Register 31
2E40	BIF_CON32	16	BIF Control Register 32
2E4A	BIF_CON37	16	BIF Control Register 37
2E4C	BIF_CON38	16	BIF Control Register 38
300E	FGADC_CUR_CON0	16	FGADC_CUR Control Register 0
3016	FGADC_CAR_CON0	16	FGADC_CAR Control Register 0
3018	FGADC_CAR_CON1	16	FGADC_CAR Control Register 1
302A	FGADC_NCAR_CON0	16	FGADC_NCAR Control Register 0
302C	FGADC_NCAR_CON1	16	FGADC_NCAR Control Register 1
3032	FGADC_IAVG_CON0	16	FGADC_IAVG Control Register 0
3034	FGADC_IAVG_CON1	16	FGADC_IAVG Control Register 1
303E	FGADC_NTER_CON0	16	FGADC_NTER Control Register 0

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Address	Name	Width	Register Function
3040	**FGADC_NTER_CON1**	16	FGADC_NTER Control Register 1
3200	**AUXADC_ADC0**	16	AUXADC ADC Register 0
3202	**AUXADC_ADC1**	16	AUXADC ADC Register 1
3204	**AUXADC_ADC2**	16	AUXADC ADC Register 2
3206	**AUXADC_ADC3**	16	AUXADC ADC Register 3
3208	**AUXADC_ADC4**	16	AUXADC ADC Register 4
320A	**AUXADC_ADC5**	16	AUXADC ADC Register 5
320C	**AUXADC_ADC6**	16	AUXADC ADC Register 6
320E	**AUXADC_ADC7**	16	AUXADC ADC Register 7
3210	**AUXADC_ADC8**	16	AUXADC ADC Register 8
3212	**AUXADC_ADC9**	16	AUXADC ADC Register 9
3214	**AUXADC_ADC10**	16	AUXADC ADC Register 10
3216	**AUXADC_ADC11**	16	AUXADC ADC Register 11
3218	**AUXADC_ADC12**	16	AUXADC ADC Register 12
321A	**AUXADC_ADC13**	16	AUXADC ADC Register 13
321C	**AUXADC_ADC14**	16	AUXADC ADC Register 14
321E	**AUXADC_ADC15**	16	AUXADC ADC Register 15
3220	**AUXADC_ADC16**	16	AUXADC ADC Register 16
3222	**AUXADC_ADC17**	16	AUXADC ADC Register 17
3224	**AUXADC_ADC18**	16	AUXADC ADC Register 18
3226	**AUXADC_ADC19**	16	AUXADC ADC Register 19
3228	**AUXADC_ADC20**	16	AUXADC ADC Register 20
322A	**AUXADC_ADC21**	16	AUXADC ADC Register 21
322C	**AUXADC_ADC22**	16	AUXADC ADC Register 22
322E	**AUXADC_ADC23**	16	AUXADC ADC Register 23
3230	**AUXADC_ADC24**	16	AUXADC ADC Register 24
3232	**AUXADC_ADC25**	16	AUXADC ADC Register 25
3234	**AUXADC_ADC26**	16	AUXADC ADC Register 26
3236	**AUXADC_ADC27**	16	AUXADC ADC Register 27
3238	**AUXADC_ADC28**	16	AUXADC ADC Register 28
323A	**AUXADC_ADC29**	16	AUXADC ADC Register 29
323C	**AUXADC_ADC30**	16	AUXADC ADC Register 30
323E	**AUXADC_ADC31**	16	AUXADC ADC Register 31
3240	**AUXADC_ADC32**	16	AUXADC ADC Register 32
3242	**AUXADC_ADC33**	16	AUXADC ADC Register 33
3244	**AUXADC_ADC34**	16	AUXADC ADC Register 34
3246	**AUXADC_ADC35**	16	AUXADC ADC Register 35
3248	**AUXADC_ADC36**	16	AUXADC ADC Register 36
324C	**AUXADC_ADC38**	16	AUXADC ADC Register 38
3256	**AUXADC_ADC43**	16	AUXADC ADC Register 43
3258	**AUXADC_ADC44**	16	AUXADC ADC Register 44
329A	**AUXADC_STA0**	16	AUXADC_STA0
329C	**AUXADC_STA1**	16	AUXADC_STA1
329E	**AUXADC_STA2**	16	AUXADC_STA2

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Address	Name	Width	Register Function
3600	AUDDEC_ANA_CON0	16	AUDDEC Control Register 0
3602	AUDDEC_ANA_CON1	16	AUDDEC Control Register 1
3604	AUDDEC_ANA_CON2	16	AUDDEC Control Register 2
3606	AUDDEC_ANA_CON3	16	AUDDEC Control Register 3
3608	AUDDEC_ANA_CON4	16	AUDDEC Control Register 4
360A	AUDDEC_ANA_CON5	16	AUDDEC Control Register 5
360C	AUDDEC_ANA_CON6	16	AUDDEC Control Register 6
360E	AUDDEC_ANA_CON7	16	AUDDEC Control Register 7
3610	AUDDEC_ANA_CON8	16	AUDDEC Control Register 8
3612	AUDDEC_ANA_CON9	16	AUDDEC Control Register 9
3614	AUDDEC_ANA_CON10	16	AUDDEC Control Register 10
3616	AUDDEC_ANA_CON11	16	AUDDEC Control Register 11
3618	AUDDEC_ANA_CON12	16	AUDDEC Control Register 12
361A	AUDDEC_ANA_CON13	16	AUDDEC Control Register 13
361C	AUDDEC_ANA_CON14	16	AUDDEC Control Register 14
361E	AUDENC_ANA_CON0	16	AUDENC Control Register 0
3620	AUDENC_ANA_CON1	16	AUDENC Control Register 1
3622	AUDENC_ANA_CON2	16	AUDENC Control Register 2
3624	AUDENC_ANA_CON3	16	AUDENC Control Register 3
3626	AUDENC_ANA_CON4	16	AUDENC Control Register 4
3628	AUDENC_ANA_CON5	16	AUDENC Control Register 5
362A	AUDENC_ANA_CON6	16	AUDENC Control Register 6
362C	AUDENC_ANA_CON7	16	AUDENC Control Register 7
362E	AUDENC_ANA_CON8	16	AUDENC Control Register 8
3630	AUDENC_ANA_CON9	16	AUDENC Control Register 9
3632	AUDENC_ANA_CON10	16	AUDENC Control Register 10
3634	AUDENC_ANA_CON11	16	AUDENC Control Register 11

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Address	Name	Width	Register Function
3636	AUDENC_ANA_CON12	16	AUDENC Control Register 12
3638	AUDENC_ANA_CON13	16	AUDENC Control Register 13
363A	AUDENC_ANA_CON14	16	AUDENC Control Register 14
363C	AUDENC_ANA_CON15	16	AUDENC Control Register 15
363E	AUDENC_ANA_CON16	16	AUDENC Control Register 16
3800	ZCD_CON0	16	ZCD Control Register 0
3802	ZCD_CON1	16	ZCD Control Register 1
3804	ZCD_CON2	16	ZCD Control Register 2
3806	ZCD_CON3	16	ZCD Control Register 3
3808	ZCD_CON4	16	ZCD Control Register 4
380A	ZCD_CON5	16	ZCD Control Register 5

0202 TEST_OUT TEST_OUT 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TEST_OUT							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TEST_OUT	Monitor

020E PGSTATUS0 Power Good Status 0 FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															STRUP_VA10_PG_STATUS	STRUP_VA12_PG_STATUS
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
1	STRUP_VA10_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
0	STRUP_VA12_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good

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0210	PGSTATUS1	Power Good Status 1	FF80

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VIO18_PG_STATUS	STRUP_VEMC_PG_STATUS	STRUP_VUFS18_PG_STATUS	STRUP_VIO28_PG_STATUS	STRUP_VSRAM_PROC_PG_STATUS	STRUP_VUSB33_PG_STATUS	STRUP_VXO22_PG_STATUS	STRUP_VXO18_PG_STATUS								
Type	RO	RO	RO	RO	RO	RO	RO	RO								
Reset	1	1	1	1	1	1	1	1								

Bit(s)	Name	Description
15	STRUP_VIO18_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
14	STRUP_VEMC_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
13	STRUP_VUFS18_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
12	STRUP_VIO28_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
11	STRUP_VSRAM_PROC_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
10	STRUP_VUSB33_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
9	STRUP_VXO22_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good
8	STRUP_VXO18_PG_STATUS	**PG status (cleared by SW)** 0: Power not good 1: Power good

0212	PSOCSTATUS	Power Source OC Status	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_VS2_OC_STATUS	STRUP_VCORE_OC_STATUS	STRUP_VGPU_OC_STATUS	STRUP_VMODEM_OC_STATUS	STRUP_VS1_OC_STATUS	STRUP_VPROC11_OC_STATUS	STRUP_VPROC12_OC_STATUS	STRUP_VDRAM1_OC_STATUS	STRUP_VDRAM2_OC_STATUS							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO							
Reset	0	0	0	0	0	0	0	0	0							

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Bit(s)	Name	Description
15	STRUP_VS2_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
14	STRUP_VCORE_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
13	STRUP_VGPU_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
12	STRUP_VMODEM_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
11	STRUP_VS1_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
10	STRUP_VPROC11_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
9	STRUP_VPROC12_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
8	STRUP_VDRAM1_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.
7	STRUP_VDRAM2_OC_STATUS	**Shutdown OC status (cleared by SW)** 0: No OC 1: OC occurs.

0216 TOPSTATUS TOP Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														HOMEKEY_DEB	PWRKEY_DEB	
Type														RO	RO	
Reset														0	0	

Bit(s)	Name	Description
2	HOMEKEY_DEB	HOMEKEY status (dynamic change with HW)
1	PWRKEY_DEB	PWRKEY status (dynamic change with HW)

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021C SMT_CON0 SMT_CON0 007C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_SMT_SCP_VREQ_VAO	RG_SMT_RTC_32K1V8_1	RG_SMT_RTC_32K1V8_0	RG_SMT_SRCLKEN_IN1	RG_SMT_SRCLKEN_IN0	RG_SMT_HOMEKEY	RG_SMT_WDTRSTB_IN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										1	1	1	1	1	0	0

Bit(s)	Name	Description
6	RG_SMT_SCP_VREQ_VAO	**SMT** 0: Disable 1: Enable
5	RG_SMT_RTC_32K1V8_1	**SMT** 0: Disable 1: Enable
4	RG_SMT_RTC_32K1V8_0	**SMT** 0: Disable 1: Enable
3	RG_SMT_SRCLKEN_IN1	**SMT** 0: Disable 1: Enable
2	RG_SMT_SRCLKEN_IN0	**SMT** 0: Disable 1: Enable
1	RG_SMT_HOMEKEY	**SMT** 0: Disable 1: Enable
0	RG_SMT_WDTRSTB_IN	**SMT** 0: Disable 1: Enable

021E SMT_CON1 SMT_CON1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_SMT_VOW_CLK_MISO	RG_SMT_AUD_DAT_MISO	RG_SMT_AUD_DAT_MOSI	RG_SMT_AUD_CLK	RG_SMT_SPI_MISO	RG_SMT_SPI_MOSI	RG_SMT_SPI_CSN	RG_SMT_SPI_CLK
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	RG_SMT_VOW_CLK_MISO	**SMT** 0: Disable 1: Enable
6	RG_SMT_AUD_DA	**SMT**

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Bit(s)	Name	Description
	T_MISO	0: Disable 1: Enable
5	RG_SMT_AUD_DAT_MOSI	**SMT** 0: Disable 1: Enable
4	RG_SMT_AUD_CLK	**SMT** 0: Disable 1: Enable
3	RG_SMT_SPI_MISO	**SMT** 0: Disable 1: Enable
2	RG_SMT_SPI_MOSI	**SMT** 0: Disable 1: Enable
1	RG_SMT_SPI_CSN	**SMT** 0: Disable 1: Enable
0	RG_SMT_SPI_CLK	**SMT** 0: Disable 1: Enable

044C **TOP_CLKSQ** **TOP_CLKSQ Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_CLKSQ_EN_VA18**															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VA18	**Status of CLKSQ** 0: Disable 1: Enable

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0452 **TOP_CLKSQ_RTC** **TOP_CLKSQ_RTC Register** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CLKSQ_EN_VDIG18															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VDIG18	**Status of CLKSQ_RTC** 0: Disable 1: Enable

0458 **TOP_CLK_TRIM** **TOP_CLK_TRIM Register** **70F8**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DA_OSC_75K_TRIM														
Type		RO														
Reset		1	1	1	0	0	0									

Bit(s)	Name	Description
14:9	DA_OSC_75K_TRIM	75kHz OSC trimming bit

060E **TOP_RST_MISC** **Reset Control Misc** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_WDTRSTB_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_WDTRSTB_EN	**WDTRSTB (external watchdog) reset from AP** 1'b0: Disable 1'b1: Enable

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0C4E **RG_SPI_CON3** **SPI Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_CMD0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_CMD0	Newest write command to MT6355

0C50 **RG_SPI_CON4** **SPI Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_CMD1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_CMD1	Write command to MT6355 before record_cmd0

0C52 **RG_SPI_CON5** **SPI Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_CMD2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_CMD2	Write command to MT6355 before record_cmd1

0C54 **RG_SPI_CON6** **SPI Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_WDATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_WDATA0	Newest write data to MT6355

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0C56 RG_SPI_CON7 SPI Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_WDATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_WDATA1	Write data to MT6355 before record_wdata0

0C58 RG_SPI_CON8 SPI Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RECORD_WDATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RECORD_WDATA2	Write data to MT6355 before record_wdata1

0E08 STRUP_CON4 STRUP Control Register N4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_OSC_EN		JUST_SMART_RST													
Type	RO		RO													
Reset	0		0													

Bit(s)	Name	Description
15	DA_QI_OSC_EN	**Enables internal oscillator** 0: disable 1: enable
13	JUST_SMART_RST	**Smart reset indicator**

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0E1A **STRUP_CON13** **STRUP Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_STRUP_PWRKEY_COUNT_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_STRUP_PWRKEY_COUNT_RESET	**Resets long press shut-down counter** 1'b1: reset long press counter 1'b0: no reset long press counter

0E2C **STRUP_ANA_CON1** **STRUP_ANA Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RGS_ANA_CHIP_ID														
Type		RO														
Reset		0	0	0												

Bit(s)	Name	Description
14:12	RGS_ANA_CHIP_ID	Chip ID

0E2E **PPCCTL0** **PPC Control 0 Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_USBDL_MODE				RG_PWRHOLD
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	RG_USBDL_MODE	**Disables BWDT in USBDL mode** 0: Normal mode 1: USBDL mode -> disable BWDT
0	RG_PWRHOLD	**Power hold** 0->1: Power hold 1->0: Power down

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100C	BUCK_OC_CONo	BUCK_OC Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_BUCK_VPA_OC_SDN_STATUS	RG_BUCK_VS2_OC_SDN_STATUS	RG_BUCK_VS1_OC_SDN_STATUS	RG_BUCK_VMODEM_OC_SDN_STATUS	RG_BUCK_VDRAM2_OC_SDN_STATUS	RG_BUCK_VDRAM1_OC_SDN_STATUS	RG_BUCK_VGPU_OC_SDN_STATUS	RG_BUCK_VCORE_OC_SDN_STATUS	RG_BUCK_VPROC12_OC_SDN_STATUS	RG_BUCK_VPROC11_OC_SDN_STATUS
Type							RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	RG_BUCK_VPA_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
8	RG_BUCK_VS2_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
7	RG_BUCK_VS1_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
6	RG_BUCK_VMODEM_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
5	RG_BUCK_VDRAM2_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
4	RG_BUCK_VDRAM1_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
3	RG_BUCK_VGPU_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
2	RG_BUCK_VCORE_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
1	RG_BUCK_VPROC12_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.
0	RG_BUCK_VPROC11_OC_SDN_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs.

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101A **BUCK_VPROC11_CON0** **BUCK VPROC11 CONTROL 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VPROC11_LP	RG_BUCK_VPROC11_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VPROC11_LP	**Enter low power mode** Valid once RG_BUCK_VPROC11_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VPROC11_EN	**Enable control (SW mode)** Valid once RG_BUCK_VPROC11_SW_OP_EN = 1'b1. 0: Off 1: On

101C **BUCK_VPROC11_CON1** **BUCK VPROC11 CONTROL 1** **0037**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC11_VOSEL						
Type										RW						
Reset										0	1	1	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC11_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.40625V + 6.25mV*VOSEL

101E **BUCK_VPROC11_CON2** **BUCK VPROC11 CONTROL 2** **0037**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC11_VOSEL_SLEEP						
Type										RW						
Reset										0	1	1	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC11_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VPROC11_VSLEEP_SEL VOUT = 0.40625V + 6.25mV*VOSEL

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103C	BUCK_VPROC12_CON0	BUCK VPROC12 CONTROL 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VPROC12_LP	RG_BUCK_VPROC12_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VPROC12_LP	**Enter low power mode** Valid once RG_BUCK_VPROC12_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VPROC12_EN	**Enable control (SW mode)** Valid once RG_BUCK_VPROC12_SW_OP_EN = 1'b1. 0: Off 1: On

103E	BUCK_VPROC12_CON1	BUCK VPROC12 CONTROL 1	0037

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC12_VOSEL						
Type										RW						
Reset										0	1	1	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC12_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.40625V + 6.25mV*VOSEL

1040	BUCK_VPROC12_CON2	BUCK VPROC12 CONTROL 2	0037

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VPROC12_VOSEL_SLEEP						
Type										RW						
Reset										0	1	1	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VPROC12_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VPROC12_VSLEEP_SEL . VOUT = 0.40625V + 6.25mV*VOSEL

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105E **BUCK_VCORE_CON0** **BUCK VCORE CONTROL 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VCORE_LP	RG_BUCK_VCORE_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VCORE_LP	**Enter low power mode** Valid once RG_BUCK_VCORE_SW_OP_EN = 1'b1 0: No LP 1: LP
0	RG_BUCK_VCORE_EN	**Enable control (SW mode)** Valid once RG_BUCK_VCORE_SW_OP_EN = 1'b1 0: Off 1: On

1060 **BUCK_VCORE_CON1** **BUCK VCORE CONTROL 1** **0037**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VCORE_VOSEL						
Type										RW						
Reset										0	1	1	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VCORE_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.40625V + 6.25mV*VOSEL

1062 **BUCK_VCORE_CON2** **BUCK VCORE CONTROL 2** **0037**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VCORE_VOSEL_SLEEP						
Type										RW						
Reset										0	1	1	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VCORE_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VCORE_VSLEEP_SEL. VOUT = 0.40625V + 6.25mV*VOSEL

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1082	BUCK_VGPU_CON0	BUCK VGPU CONTROL 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VGPU_LP	RG_BUCK_VGPU_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VGPU_LP	**Enter low power mode** Valid once RG_BUCK_VGPU_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VGPU_EN	**Enable control (SW mode)** Valid once RG_BUCK_VGPU_SW_OP_EN = 1'b1. 0: Off 1: On

1084	BUCK_VGPU_CON1	BUCK VGPU CONTROL 1	0027

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VGPU_VOSEL						
Type										RW						
Reset										0	1	0	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VGPU_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.40625V + 6.25mV*VOSEL

1086	BUCK_VGPU_CON2	BUCK VGPU CONTROL 2	0027

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VGPU_VOSEL_SLEEP						
Type										RW						
Reset										0	1	0	0	1	1	1

Bit(s)	Name	Description
6:0	RG_BUCK_VGPU_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VGPU_VSLEEP_SEL. VOUT = 0.40625V + 6.25mV*VOSEL

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10A4 BUCK_VDRAM1_CON0 BUCK VDRAM1 Control 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VDRAM1_LP	RG_BUCK_VDRAM1_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VDRAM1_LP	**Enter low power mode** Valid once RG_BUCK_VDRAM1_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VDRAM1_EN	**Enable control (SW mode)** Valid once RG_BUCK_VDRAM1_SW_OP_EN = 1'b1. 0: Off 1: On

10A6 BUCK_VDRAM1_CON1 BUCK VDRAM1 Control 1 0061

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VDRAM1_VOSEL						
Type										RW						
Reset										1	1	0	0	0	0	1

Bit(s)	Name	Description
6:0	RG_BUCK_VDRAM1_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.51875V + 6.25mV*VOSEL

10A8 BUCK_VDRAM1_CON2 BUCK VDRAM1 Control 2 0061

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VDRAM1_VOSEL_SLEEP						
Type										RW						
Reset										1	1	0	0	0	0	1

Bit(s)	Name	Description
6:0	RG_BUCK_VDRAM1_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VDRAM1_VSLEEP_SEL. VOUT = 0.51875V + 6.25mV*VOSEL

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10C6 BUCK_VDRAM2_CON0 BUCK VDRAM2 Control 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VDRAM2_LP	RG_BUCK_VDRAM2_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VDRAM2_LP	**Enter low power mode** Valid once RG_BUCK_VDRAM2_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VDRAM2_EN	**Enable control (SW mode)** Valid once RG_BUCK_VDRAM2_SW_OP_EN = 1'b1. 0: Off 1: On

10C8 BUCK_VDRAM2_CON1 BUCK VDRAM2 Control 1 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VDRAM2_VOSEL						
Type										RW						
Reset										0	1	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VDRAM2_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.4V + 6.25mV*VOSEL

10CA BUCK_VDRAM2_CON2 BUCK VDRAM2 Control 2 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VDRAM2_VOSEL_SLEEP						
Type										RW						
Reset										0	1	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VDRAM2_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VDRAM2_VSLEEP_SEL. VOUT = 0.4V + 6.25mV*VOSEL

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10E8	BUCK_VMODEM_CON0	BUCK VMODEM Control 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VMODEM_LP	RG_BUCK_VMODEM_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VMODEM_LP	**Enter low power mode** Valid once RG_BUCK_VMODEM_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VMODEM_EN	**Enable control (SW mode)** Valid once RG_BUCK_VMODEM_SW_OP_EN = 1'b1. 0: Off 1: On

10EA	BUCK_VMODEM_CON1	BUCK VMODEM Control 1	0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VMODEM_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VMODEM_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.4V + 6.25mV*VOSEL

10EC	BUCK_VMODEM_CON2	BUCK VMODEM Control 2	0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_BUCK_VMODEM_VOSEL_SLEEP						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_BUCK_VMODEM_VOSEL_SLEEP	**Selects VOUT in sleep mode** Give the same voltage as RG_VMODEM_VSLEEP_SEL. VOUT = 0.4V + 6.25mV*VOSEL

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1112	BUCK_VS1_CON0	BUCK VS1 Control 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VS1_LP	RG_BUCK_VS1_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VS1_LP	**Enter low power mode** Valid once RG_BUCK_VS1_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VS1_EN	**Enable control (SW mode)** Valid once RG_BUCK_VS1_SW_OP_EN = 1'b1. 0: Off 1: On

113C	BUCK_VS2_CON0	BUCK VS2 Control 0	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_BUCK_VS2_LP	RG_BUCK_VS2_EN
Type															RW	RW
Reset															0	1

Bit(s)	Name	Description
1	RG_BUCK_VS2_LP	**Enter low power mode** Valid once RG_BUCK_VS2_SW_OP_EN = 1'b1. 0: No LP 1: LP
0	RG_BUCK_VS2_EN	**Enable control (SW mode)** Valid once RG_BUCK_VS2_SW_OP_EN = 1'b1. 0: Off 1: On

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1166 **BUCK_VPA_CON0** **BUCK VPA Control 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_BUCK_VPA_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_BUCK_VPA_EN	Enable control (SW mode)

1168 **BUCK_VPA_CON1** **BUCK VPA Control 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**RG_BUCK_VPA_VOSEL**					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	RG_BUCK_VPA_VOSEL	**Selects VOUT in normal mode (SW mode)** VOUT = 0.5V + 50mV*VOSEL

1204 **SMPS_ANA_CON2** **SMPS Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**RG_VCORE_SLEEP_VOLTAGE**														
Type		RW														
Reset		0	0													

Bit(s)	Name	Description
14:13	RG_VCORE_SLEEP_VOLTAGE	**Selects sleep mode voltage** For MT6757 family: 00: 0.568V, default 01: 0.625V 10: 0.65V 11: 0.75V For MT6758: 00: 0.55, default 01: 0.6 10: 0.7 11: 0.8

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1206	SMPS_ANA_CON3	SMPS Control Register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VDRAM1_SLEEP_VOLTAGE													
Type			RW													
Reset			0													

Bit(s)	Name	Description
13	RG_VDRAM1_SLEEP_VOLTAGE	**Selects sleep mode voltage** 0: 1.125V 1: 1.225V

1208	SMPS_ANA_CON4	SMPS Control Register 4	A000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VMODEM_SLEEP_VOLTAGE															
Type	RW															
Reset	1	0	1													

Bit(s)	Name	Description
15:13	RG_VMODEM_SLEEP_VOLTAGE	**Selects sleep mode voltage** 000: 0.40V 001: 0.45V 010: 0.50V 011: 0.525V 100: 0.55V 101: 0.568V (default) 110: 0.60V 111: 0.65V

120A	SMPS_ANA_CON5	SMPS Control Register 5	4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VGPU_SLEEP_VOLTAGE														
Type		RW														
Reset		1	0													

Bit(s)	Name	Description
14:13	RG_VGPU_SLEEP_	**Selects sleep mode voltage**

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Bit(s)	Name	Description
	VOLTAGE	For MT6759/MT6757 family: 00: 0.45V 01: 0.50V 10: 0.568V, default 11: 0.60V For MT6758: 00: 0.45 01: 0.5 10: 0.65 11: 0.65

1212 **SMPS_ANA_CON9** **SMPS Control Register 9** **2000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VPROC11_SLEEP_VOLTAGE														
Type		RW														
Reset		0	1													

Bit(s)	Name	Description
14:13	RG_VPROC11_SLEEP_VOLTAGE	**Selects sleep mode voltage** 00: 0.5V 01: 0.568V (MT6759) 10: 0.6V (MT6757 family/MT6758) 11: 0.65V

1214 **SMPS_ANA_CON10** **SMPS Control Register 10** **2000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VPROC12_SLEEP_VOLTAGE														
Type		RW														
Reset		0	1													

Bit(s)	Name	Description
14:13	RG_VPROC12_SLEEP_VOLTAGE	**Selects sleep mode voltage** 00: 0.5V 01: 0.568V (MT6759) 10: 0.6V(MT6757 family/MT6758) 11: 0.65V

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1216 **SMPS_ANA_CON11** **SMPS Control Register 11** **2000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VSRAM_PROC_SLEEP_VOLTAGE														
Type		RW														
Reset		0	1													

Bit(s)	Name	Description
14:13	RG_VSRAM_PROC_SLEEP_VOLTAGE	**Selects sleep mode voltage** 00: 0.6V (MT6757 family) 01: 0.65V (MT6759) 10: 0.7V 11: 0.8V

1218 **SMPS_ANA_CON12** **SMPS Control Register 12** **2000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VSRAM_CORE_SLEEP_VOLTAGE															
Type	RW															
Reset	0	0	1													

Bit(s)	Name	Description
15:13	RG_VSRAM_CORE_SLEEP_VOLTAGE	**Selects sleep mode voltage** 000: 0.6V (MT6757 family) 001: 0.65V (MT6759) 010: 0.7V 011: 0.8V 1XX: NA

121A **SMPS_ANA_CON13** **SMPS Control Register 13** **2000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VSRAM_GPU_SLEEP_VOLTAGE														
Type		RW														
Reset		0	1													

Bit(s)	Name	Description
14:13	RG_VSRAM_GPU_SLEEP_VOLTAGE	**Selects sleep mode voltage** 00: 0.6V 01: 0.65V (target) 10: 0.7V 11: 0.8V

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121C SMPS_ANA_CON14 SMPS Control Register 14 2000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VSRAM_MD_SLEEP_VOLTAGE															
Type	RW															
Reset	0	0	1													

Bit(s)	Name	Description
15:13	RG_VSRAM_MD_SLEEP_VOLTAGE	**Selects sleep mode voltage** 000: 0.6V 001: 0.65V (default) 010: 0.7V 011: 0.8V 1XX: NA

160E LDO_VIO28_CON1 LDO VIO28 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIO28_EN							DA_QI_VIO28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VIO28_EN	**VIO28 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VIO28_MODE	**VIO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1622 LDO_VIO18_CON1 LDO VIO18 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIO18_EN							DA_QI_VIO18_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_QI_VIO18_EN	**VIO18 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VIO18_MODE	**VIO18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1636 **LDO_VUFS18_CON1** **LDO VUFS18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VUFS18_EN							DA_QI_VUFS18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VUFS18_EN	**VUFS18 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VUFS18_MODE	**VUFS18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

164C **LDO_VA10_CON2** **LDO VA10 Control Register 2** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VA10_EN							DA_QI_VA10_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VA10_EN	**VA10 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VA10_MODE	**VA10 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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1660	LDO_VA12_CON1	LDO VA12 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VA12_EN							DA_QI_VA12_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VA12_EN	**VA12 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VA12_MODE	**VA12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1674	LDO_VA18_CON1	LDO VA18 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VA18_EN							DA_QI_VA18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VA18_EN	**VA18 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VA18_MODE	**VA18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

168A	LDO_VUSB33_CON1	LDO VUSB33 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VUSB33_EN							DA_QI_VUSB33_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_QI_VUSB33_EN	**VUSB33 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VUSB33_MODE	**VUSB33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

169E **LDO_VEMC_CON1** **LDO VEMC Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VEMC_EN							DA_QI_VEMC_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VEMC_EN	**VEMC enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VEMC_MODE	**VEMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

16B2 **LDO_VXO22_CON1** **LDO VXO22 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VXO22_EN							DA_QI_VXO22_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VXO22_EN	**VXO22 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VXO22_MODE	**VXO22 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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16C6 **LDO_VXO18_CON1** **LDO VXO18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VXO18_EN							DA_QI_VXO18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VXO18_EN	**VXO18 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VXO18_MODE	**VXO18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

16CC **LDO_VSIM1_CON0** **LDO VSIM1 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VSIM1_LP	RG_LDO_VSIM1_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VSIM1_LP	**Enter low power mode** Valid once RG_LDO_VSIM1_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VSIM1_EN	**Enable control (SW mode)** Valid once RG_LDO_VSIM1_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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16CE LDO_VSIM1_OP_EN LDO VSIM1 Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VSIM1_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VSIM1_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

16DA LDO_VSIM1_CON1 LDO VSIM1 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSIM1_EN							DA_QI_VSIM1_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VSIM1_EN	**VSIM1 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VSIM1_MODE	**VSIM1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

16E0 LDO_VSIM2_CON0 LDO VSIM2 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VSIM2_LP	RG_LDO_VSIM2_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VSIM2_L	**Enter low power mode**

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Bit(s)	Name	Description
	P	Valid once RG_LDO_VSIM2_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VSIM2_EN	**Enable control (SW mode)** Valid once RG_LDO_VSIM2_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

16E2 LDO_VSIM2_OP_EN LDO VSIM2 Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VSIM2_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VSIM2_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

16EE LDO_VSIM2_CON1 LDO VSIM2 Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSIM2_EN							DA_QI_VSIM2_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VSIM2_EN	**VSIM2 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VSIM2_MODE	**VSIM2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

16F4 LDO_VCAMD1_CON0 LDO VCAMD1 Control Register 0 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMD1_LP	RG_LDO_VCAMD1_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMD1_LP	**Enter low power mode** Valid once RG_LDO_VCAMD1_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMD1_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMD1_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

16F6 **LDO_VCAMD1_OP_EN** **LDO VCAMD1 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMD1_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMD1_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1702 **LDO_VCAMD1_CON1** **LDO VCAMD1 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMD1_EN							DA_QI_VCAMD1_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	DA_QI_VCAMD1_EN	**VCAMD1 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCAMD1_MODE	**VCAMD1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1708 **LDO_VCAMD2_CON0** **LDO VCAMD2 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMD2_LP	RG_LDO_VCAMD2_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMD2_LP	**Enter low power mode** Valid once RG_LDO_VCAMD2_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMD2_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMD2_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

170A **LDO_VCAMD2_OP_EN** **LDO VCAMD2 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMD2_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMD2_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

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1716 **LDO_VCAMD2_CON1** **LDO VCAMD2 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMD2_EN							DA_QI_VCAMD2_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VCAMD2_EN	**VCAMD2 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCAMD2_MODE	**VCAMD2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

171C **LDO_VCAMIO_CON0** **LDO VCAMIO Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMIO_LP	RG_LDO_VCAMIO_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMIO_LP	**Enter low power mode** Valid once RG_LDO_VCAMIO_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMIO_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMIO_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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171E	LDO_VCAMIO_OP_EN	LDO VCAMIO Operation Enable	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMIO_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMIO_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

172A	LDO_VCAMIO_CON1	LDO VCAMIO Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMIO_EN							DA_QI_VCAMIO_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VCAMIO_EN	**VCAMIO enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCAMIO_MODE	**VCAMIO low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1730	LDO_VMIPI_CON0	LDO VMIPI Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMIPI_LP	RG_LDO_VMIPI_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1	RG_LDO_VMIPI_LP	**Enter low power mode** Valid once RG_LDO_VMIPI_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VMIPI_EN	**Enable control (SW mode)** Valid once RG_LDO_VMIPI_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1732	LDO_VMIPI_OP_EN	LDO VMIPI Operation Enable	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VMIPI_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMIPI_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

173E	LDO_VMIPI_CON1	LDO VMIPI Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMIPI_EN							DA_QI_VMIPI_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VMIPI_EN	**VMIPI enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VMIPI_MODE	**VMIPI low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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1744 LDO_VGP_CON0 LDO VGP Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VGP_LP	RG_LDO_VGP_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VGP_LP	**Enter low power mode** Valid once RG_LDO_VGP_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VGP_EN	**Enable control (SW mode)** Valid once RG_LDO_VGP_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1746 LDO_VGP_OP_EN LDO VGP Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VGP_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VGP_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1752 LDO_VGP_CON1 LDO VGP Control Register 1 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VGP_EN							DA_QI_VGP_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	DA_QI_VGP_EN	**VGP enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VGP_MODE	**VGP low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1758 LDO_VCN33_CON0_BT LDO VCN33 bt Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN33_LP	RG_LDO_VCN33_EN_BT
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN33_LP	**Enter low power mode** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN33_EN_BT	**Enable control (SW mode)** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

175A LDO_VCN33_OP_EN LDO VCN33 Operation Enable 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN33_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN33_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

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1766 **LDO_VCN33_CON0_WIFI** **LDO VCN33 wifi Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN33_EN_WIFI
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_LDO_VCN33_EN_WIFI	**Enable control (SW mode)** Valid once RG_LDO_VCN33_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1768 **LDO_VCN33_CON1** **LDO VCN33 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN33_EN							DA_QI_VCN33_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VCN33_EN	**VCN33 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCN33_MODE	**VCN33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

176E **LDO_VCN18_CON0** **LDO VCN18 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN18_LP	RG_LDO_VCN18_EN
Type															RW	RW
Reset															0	0

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Bit(s)	Name	Description
1	RG_LDO_VCN18_LP	**Enter low power mode** Valid once RG_LDO_VCN18_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN18_EN	**Enable control (SW mode)** Valid once RG_LDO_VCN18_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1770 **LDO_VCN18_OP_EN** **LDO VCN18 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN18_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN18_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

177C **LDO_VCN18_CON1** **LDO VCN18 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN18_EN							DA_QI_VCN18_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VCN18_EN	**VCN18 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCN18_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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1782	LDO_VCN28_CON0	LDO VCN28 Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCN28_LP	RG_LDO_VCN28_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCN28_LP	**Enter low power mode** Valid once RG_LDO_VCN28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCN28_EN	**Enable control (SW mode)** Valid once RG_LDO_VCN28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1784	LDO_VCN28_OP_EN	LDO VCN28 Operation Enable	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCN28_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCN28_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1790	LDO_VCN28_CON1	LDO VCN28 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN28_EN							DA_QI_VCN28_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_QI_VCN28_EN	**VCN28 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCN28_MODE	**VCN28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1796 **LDO_VBIF28_CON0** **LDO VBIF28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VBIF28_LP	RG_LDO_VBIF28_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VBIF28_LP	**Enter low power mode** Valid once RG_LDO_VBIF28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VBIF28_EN	**Enable control (SW mode)** Valid once RG_LDO_VBIF28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1798 **LDO_VBIF28_OP_EN** **LDO VBIF28 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VBIF28_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VBIF28_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

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17A4 **LDO_VBIF28_CON1** **LDO VBIF28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VBIF28_EN							DA_QI_VBIF28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VBIF28_EN	**VBIF28 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VBIF28_MODE	**VBIF28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

17AA **LDO_VTCXO24_CON0** **LDO VTCXO24 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VTCXO24_LP	RG_LDO_VTCXO24_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VTCXO24_LP	**Enter low power mode** Valid once RG_LDO_VTCXO24_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VTCXO24_EN	**Enable control (SW mode)** Valid once RG_LDO_VTCXO24_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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17AC **LDO_VTCXO24_OP_EN** **LDO VTCXO24 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_LDO_VTCXO24_SW_OP_EN**
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VTCXO24_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

17B8 **LDO_VTCXO24_CON1** **LDO VTCXO24 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VTCXO24_EN**							**DA_QI_VTCXO24_MODE**								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VTCXO24_EN	**VTCXO24 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VTCXO24_MODE	**VTCXO24 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

17BE **LDO_VLDO28_CON0_AF** **LDO VLDO28 AF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_LDO_VLDO28_LP**	**RG_LDO_VLDO28_EN_AF**
Type															RW	RW
Reset															0	0

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Bit(s)	Name	Description
1	RG_LDO_VLDO28_LP	**Enter low power mode** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VLDO28_EN_AF	**Enable control (SW mode)** Valid once RG_LDO_VLDO28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

17C0 **LDO_VLDO28_OP_EN** **LDO VLDO28 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VLDO28_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VLDO28_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

17CE **LDO_VLDO28_CON1** **LDO VLDO28 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VLDO28_EN							DA_QI_VLDO28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VLDO28_EN	**VLDO28 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VLDO28_MODE	**VLDO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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17D4 **LDO_VGP2_CON0** **LDO VGP2 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VGP2_LP	RG_LDO_VGP2_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VGP2_LP	**Enter low power mode** Valid once RG_LDO_VGP2_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VGP2_EN	**Enable control (SW mode)** Valid once RG_LDO_VGP2_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

17D6 **LDO_VGP2_OP_EN** **LDO VGP2 Operation Enable** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VGP2_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VGP2_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

17E2 **LDO_VGP2_CON1** **LDO VGP2 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VGP2_EN							DA_QI_VGP2_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	DA_QI_VGP2_EN	**VGP2 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VGP2_MODE	**VGP2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1800 **LDO_VFE28_CON0** **LDO VFE28 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VFE28_LP	RG_LDO_VFE28_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VFE28_LP	**Enter low power mode** Valid once RG_LDO_VFE28_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VFE28_EN	**Enable control (SW mode)** Valid once RG_LDO_VFE28_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1802 **LDO_VFE28_OP_EN** **LDO VFE28 OPERATION ENABLE** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VFE28_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VFE28_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

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180E	LDO_VFE28_CON1	LDO VFE28 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VFE28_EN							DA_QI_VFE28_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VFE28_EN	**VFE28 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VFE28_MODE	**VFE28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1814	LDO_VMCH_CON0	LDO VMCH Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMCH_LP	RG_LDO_VMCH_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMCH_LP	**Enter low power mode** Valid once RG_LDO_VMCH_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VMCH_EN	**Enable control (SW mode)** Valid once RG_LDO_VMCH_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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1816 **LDO_VMCH_OP_EN** **LDO VMCH OPERATION ENABLE** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VMCH_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMCH_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1822 **LDO_VMCH_CON1** **LDO VMCH Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMCH_EN							DA_QI_VMCH_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VMCH_EN	**VMCH enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VMCH_MODE	**VMCH low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1828 **LDO_VMC_CON0** **LDO VMC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VMC_LP	RG_LDO_VMC_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VMC_LP	**Enter low power mode**

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Bit(s)	Name	Description
		Valid once RG_LDO_VMC_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VMC_EN	**Enable control (SW mode)** Valid once RG_LDO_VMC_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

182A **LDO_VMC_OP_EN** **LDO VMC OPERATION ENABLE** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VMC_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VMC_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1836 **LDO_VMC_CON1** **LDO VMC Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMC_EN							DA_QI_VMC_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VMC_EN	**VMC enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VMC_MODE	**VMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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183C	LDO_VRF18_1_CON0	LDO VRF18_1 Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF18_1_LP	RG_LDO_VRF18_1_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF18_1_LP	**Enter low power mode** Valid once RG_LDO_VRF18_1_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF18_1_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF18_1_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

183E	LDO_VRF18_1_OP_EN	LDO VRF18_1 OPERATION ENABLE	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF18_1_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VRF18_1_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

184A	LDO_VRF18_1_CON1	LDO VRF18_1 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRF18_1_EN							DA_QI_VRF18_1_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_QI_VRF18_1_EN	**VRF18_1 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VRF18_1_MODE	**VRF18_1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1850 **LDO_VRF18_2_CON0** **LDO VRF18_2 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF18_2_LP	RG_LDO_VRF18_2_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF18_2_LP	**Enter low power mode** Valid once RG_LDO_VRF18_2_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF18_2_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF18_2_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

1852 **LDO_VRF18_2_OP_EN** **LDO VRF18_2 OPERATION ENABLE** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF18_2_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VRF18_2_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

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185E **LDO_VRF18_2_CON1** **LDO VRF18_2 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRF18_2_EN							DA_QI_VRF18_2_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VRF18_2_EN	**VRF18_2 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VRF18_2_MODE	**VRF18_2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1864 **LDO_VRF12_CON0** **LDO VRF12 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VRF12_LP	RG_LDO_VRF12_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VRF12_LP	**Enter low power mode** Valid once RG_LDO_VRF12_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VRF12_EN	**Enable control (SW mode)** Valid once RG_LDO_VRF12_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

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1866	LDO_VRF12_OP_EN	LDO VRF12 OPERATION ENABLE	0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VRF12_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VRF12_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1872	LDO_VRF12_CON1	LDO VRF12 Control Register 1	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRF12_EN							DA_QI_VRF12_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VRF12_EN	**VRF12 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VRF12_MODE	**VRF12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1878	LDO_VCAMA1_CON0	LDO VCAMA1 Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMA1_LP	RG_LDO_VCAMA1_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1	RG_LDO_VCAMA1_LP	**Enter low power mode** Valid once RG_LDO_VCAMA1_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMA1_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMA1_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

187A **LDO_VCAMA1_OP_EN** **LDO VCAMA1 OPERATION ENABLE** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMA1_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMA1_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

1886 **LDO_VCAMA1_CON1** **LDO VCAMA1 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMA1_EN							DA_QI_VCAMA1_MODE								
Type	RO							RO								
Reset	0							0								

Bit(s)	Name	Description
15	DA_QI_VCAMA1_EN	**VCAMA1 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCAMA1_MODE	**VCAMA1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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188C **LDO_VCAMA2_CON0** **LDO VCAMA2 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_LDO_VCAMA2_LP	RG_LDO_VCAMA2_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_LDO_VCAMA2_LP	**Enter low power mode** Valid once RG_LDO_VCAMA2_SW_OP_EN = 1'b1. 1'b0: No LP 1'b1: LP
0	RG_LDO_VCAMA2_EN	**Enable control (SW mode)** Valid once RG_LDO_VCAMA2_SW_OP_EN = 1'b1. 1'b0: Off 1'b1: On

188E **LDO_VCAMA2_OP_EN** **LDO VCAMA2 OPERATION ENABLE** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_LDO_VCAMA2_SW_OP_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_LDO_VCAMA2_SW_OP_EN	**Enables SW operation** 1'b0: Disable 1'b1: Enable

189A **LDO_VCAMA2_CON1** **LDO VCAMA2 Control Register 1** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMA2_EN							DA_QI_VCAMA2_MODE								
Type	RO							RO								
Reset	0							0								

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Bit(s)	Name	Description
15	DA_QI_VCAMA2_EN	**VCAMA2 enable status** 1'b1: Enable 1'b0: Disable
8	DA_QI_VCAMA2_MODE	**VCAMA2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

18A2 **VRTC_CON0** **VRTC Control Register 0** **8002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRTC_EN															
Type	RO															
Reset	1															

Bit(s)	Name	Description
15	DA_QI_VRTC_EN	VRTC enable status

18BE **LDO_VSRAM_PROC_CON3** **LDO VSRAM_PROC Control Register 3** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_QI_VSRAM_PROC_MODE								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_QI_VSRAM_PROC_MODE	**VSRAM_PROC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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18C6 **LDO_VSRAM_PROC_DBG1** **LDO VSRAM_PROC DEBUG 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_QI_VSRAM_PROC_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_QI_VSRAM_PROC_EN	VSRAM_PROC enable status

18DE **LDO_VSRAM_CORE_CON3** **LDO VSRAM_CORE Control Register 3** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_QI_VSRAM_CORE_MODE								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_QI_VSRAM_CORE_MODE	**VSRAM_CORE low power mode status** 1'b0: Normal mode 1'b1: Low power mode

18E6 **LDO_VSRAM_CORE_DBG1** **LDO VSRAM_CORE DEBUG 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_QI_VSRAM_CORE_EN
Type																RO
Reset																0

Bit(s)	Name	Description

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Bit(s)	Name	Description
0	DA_QI_VSRAM_CORE_EN	VSRAM_CORE enable status

18FE **LDO_VSRAM_GPU_CON3** **LDO VSRAM_GPU Control Register 3** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_QI_VSRAM_GPU_MODE								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_QI_VSRAM_GPU_MODE	**VSRAM_GPU low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1906 **LDO_VSRAM_GPU_DBG1** **LDO VSRAM_GPU DEBUG 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_QI_VSRAM_GPU_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_QI_VSRAM_GPU_EN	VSRAM_GPU enable status

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191E	LDO_VSRAM_MD_CON3	LDO VSRAM_MD Control Register 3	0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_QI_VSRAM_MD_MODE								
Type								RO								
Reset								0								

Bit(s)	Name	Description
8	DA_QI_VSRAM_MD_MODE	**VSRAM_MD low power mode status** 1'b0: Normal mode 1'b1: Low power mode

1926	LDO_VSRAM_MD_DBG1	LDO VSRAM_MD DEBUG 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DA_QI_VSRAM_MD_EN
Type																RO
Reset																0

Bit(s)	Name	Description
0	DA_QI_VSRAM_MD_EN	VSRAM_MD enable status

1A00	ALDO_ANA_CON0	ALDO Control Register 0	0A00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VFE28_VOSEL								RG_VFE28_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VFE28_VOSEL	**Selects output voltage** 4'b1010: 2.8V
3:0	RG_VFE28_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV

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Bit(s)	Name	Description
		4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110:+60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A04 **ALDO_ANA_CON2** **ALDO Control Register 2** **0508**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VTCXO24_VOSEL								RG_VTCXO24_VOCAL			
Type					RW								RW			
Reset					0	1	0	1					1	0	0	0

Bit(s)	Name	Description
11:8	RG_VTCXO24_VOSEL	**Selects output voltage** 4'b0101: 2.3V
3:0	RG_VTCXO24_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A0C **ALDO_ANA_CON6** **ALDO Control Register 6** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCN28_VOSEL								RG_VCN28_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCN28_VOSEL	**Selects output voltage** 4'b1010: 2.8V
3:0	RG_VCN28_VOCAL	**Calibrates output voltage** 4'b0000:+00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV

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Bit(s)	Name	Description
		4'b0111: +70mV 4'b1000: + 80mV 4'b1001: +90mV 4'b1010: +100mV

1A10 **ALDO_ANA_CON8** **ALDO Control Register 8** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMA1_VOSEL								RG_VCAMA1_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMA1_VOSEL	**Selects output voltage** 4'b0000: 1.8V 4'b0111: 2.5V 4'b1001: 2.7V 4'b1010 2.8V 4'b1011: 2.9V 4'b1100: 3.0V
3:0	RG_VCAMA1_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100:+40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A14 **ALDO_ANA_CON10** **ALDO Control Register 10** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMA2_VOSEL								RG_VCAMA2_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMA2_VOSEL	**Selects output voltage** 4'b0000: 1.8V 4'b0111: 2.5V 4'b1001: 2.7V 4'b1010 2.8V 4'b1011: 2.9V 4'b1100: 3.0V
3:0	RG_VCAMA2_VOCAL	**Calibrates output voltage** 4'b0000: +00mV

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Bit(s)	Name	Description
		4'b0001: +10mV 4'b0010: +20mV 4'b0011:+30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A20 **ALDO_ANA_CON16** **ALDO Control Register 16** **0A00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VBIF28_VOSEL								RG_VBIF28_VOCAL			
Type					RW								RW			
Reset					1	0	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VBIF28_VOSEL	**Selects output voltage** 4'b1010: 2.8V
3:0	RG_VBIF28_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A24 **ALDO_ANA_CON18** **ALDO Control Register 18** **0900**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VGP2_VOSEL								RG_VGP2_VOCAL			
Type					RW								RW			
Reset					1	0	0	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VGP2_VOSEL	**Selects output voltage** 4'b0000: 1.2V 4'b0001: 1.3V 4'b0010: 1.5V 4'b0100:1.8V 4'b0101: 2.0V 4'b1001: 2.8V 4'b1011: 3.0V

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Bit(s)	Name	Description
		4'b1101: 3.3V
3:0	RG_VGP2_VOCAL	**Calibrates output voltage** 4'b0000:+00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A2C **DLDO_ANA_CON2** **DLDO Control Register 2** **0406**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM1_VOSEL								RG_VSIM1_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	1	1	0

Bit(s)	Name	Description
11:8	RG_VSIM1_VOSEL	**Selects output voltage** 4'b0011: 1.7V 4'b0100: 1.8V 4'b1000: 2.7V 4'b1011: 3.0V 4'b1100: 3.1V
3:0	RG_VSIM1_VOCAL	**Calibrates output voltage** 4'b0000:+00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A30 **DLDO_ANA_CON4** **DLDO Control Register 4** **0406**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM2_VOSEL								RG_VSIM2_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					0	1	1	0

Bit(s)	Name	Description
11:8	RG_VSIM2_VOSEL	**Selects output voltage**

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Bit(s)	Name	Description
		4'b0011: 1.7V 4'b0100: 1.8V 4'b1000: 2.7V 4'b1011: 3.0V 4'b1100: 3.1V
3:0	RG_VSIM2_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A34 DLDO_ANA_CON6 DLDO Control Register 6 0900

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VLDO28_VOSEL								RG_VLDO28_VOCAL			
Type					RW								RW			
Reset					1	0	0	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VLDO28_VOSEL	**Selects output voltage** 4'b1001: 2.8V 4'b1011: 3.0V
3:0	RG_VLDO28_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A3C DLDO_ANA_CON10 DLDO Control Register 10 0B00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMC_VOSEL								RG_VMC_VOCAL			
Type					RW								RW			
Reset					1	0	1	1					0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
11:8	RG_VMC_VOSEL	**Selects output voltage** 4'b0100: 1.8V 4'b1010: 2.9V 4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VMC_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A40 DLDO_ANA_CON12 DLDO Control Register 12 0B00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMCH_VOSEL								RG_VMCH_VOCAL			
Type					RW								RW			
Reset					1	0	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VMCH_VOSEL	**Selects output voltage** 4'b1010: 2.9V 4'b1011: 3.0V 4'b1101: 3.3V
3:0	RG_VMCH_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A48 DLDO_ANA_CON16 DLDO Control Register 16 0409

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VGP_VOSEL								RG_VGP_VOCAL			
Type					RW								RW			
Reset					0	1	0	0					1	0	0	1

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Bit(s)	Name	Description
11:8	RG_VGP_VOSEL	**Selects output voltage** 4'b0010: 1.5V 4'b0011: 1.7V 4'b0100: 1.8V 4'b0101: 2.0V 4'b0110: 2.1V 4'b0111: 2.2V 4'b1001: 2.8V 4'b1101: 3.3V
3:0	RG_VGP_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A4C **SLDO20_ANA_CON0** **SLDO20 Control Register 0** **0700**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VRF18_1_VOSEL								RG_VRF18_1_VOCAL			
Type					RW								RW			
Reset					0	1	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VRF18_1_VOSEL	**Selects output voltage** 4'b0111: 1.81V
3:0	RG_VRF18_1_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A50 **SLDO20_ANA_CON2** **SLDO20 Control Register 2** **0700**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VRF18_2_VOSEL								RG_VRF18_2_VOCAL			
Type					RW								RW			
Reset					0	1	1	1					0	0	0	0

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Bit(s)	Name	Description
11:8	RG_VRF18_2_VOSEL	**Selects output voltage** 4'b0111: 1.81V
3:0	RG_VRF18_2_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A54 SLDO20_ANA_CON4 SLDO20 Control Register 4 0C00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCN18_VOSEL								RG_VCN18_VOCAL			
Type					RW								RW			
Reset					1	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCN18_VOSEL	**Selects output voltage** 4'b1100: 1.8V
3:0	RG_VCN18_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A58 SLDO20_ANA_CON6 SLDO20 Control Register 6 0C00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMIO_VOSEL								RG_VCAMIO_VOCAL			
Type					RW								RW			
Reset					1	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMIO_VOSEL	**Selects output voltage** 4'b1100:1.8V

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Bit(s)	Name	Description
3:0	RG_VCAMIO_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A5C **SLDO20_ANA_CON8** **SLDO20 Control Register 8** **0C00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VMIPI_VOSEL								RG_VMIPI_VOCAL			
Type					RW								RW			
Reset					1	1	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VMIPI_VOSEL	**Selects output voltage** 4'b1011: 1.7V 4'b1100: 1.8V 4'b1110: 2.0V 4'b1111: 2.1V
3:0	RG_VMIPI_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A6C **SLDO14_ANA_CON0** **SLDO14 Control Register 0** **0300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VRF12_VOSEL								RG_VRF12_VOCAL			
Type					RW								RW			
Reset					0	0	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VRF12_VOSEL	**Selects output voltage** 4'b0011: 1.2V
3:0	RG_VRF12_VOCAL	**Calibrates output voltage**

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Bit(s)	Name	Description
		4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A70 SLDO14_ANA_CON2 SLDO14 Control Register 2 0600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMD1_VOSEL								RG_VCAMD1_VOCAL			
Type					RW								RW			
Reset					0	1	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMD1_VOSEL	**Selects output voltage** 4'b0011: 0.9V 4'b0100: 1.0V 4'b0101: 1.1V 4'b0110: 1.2V
3:0	RG_VCAMD1_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1A74 SLDO14_ANA_CON4 SLDO14 Control Register 4 0600

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMD2_VOSEL								RG_VCAMD2_VOCAL			
Type					RW								RW			
Reset					0	1	1	0					0	0	0	0

Bit(s)	Name	Description
11:8	RG_VCAMD2_VOSEL	**Selects output voltage** 4'b0011: 0.9V 4'b0100: 1.0V 4'b0101: 1.1V 4'b0110: 1.2V

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Bit(s)	Name	Description
		4'b0111: 1.3V 4'b1001: 1.5V 4'b1100: 1.8V
3:0	RG_VCAMD2_VOCAL	**Calibrates output voltage** 4'b0000: +00mV 4'b0001: +10mV 4'b0010: +20mV 4'b0011: +30mV 4'b0100: +40mV 4'b0101: +50mV 4'b0110: +60mV 4'b0111: +70mV 4'b1000: +80mV 4'b1001: +90mV 4'b1010: +100mV

1C00 **ACCDET_CON0** **ACCDET Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUDACCDETAUXADCSWCTRL_SEL											
Type					RW											
Reset					0											

Bit(s)	Name	Description
11	AUDACCDETAUXADCSWCTRL_SEL	**Controls DA_NI_AUDACCDETAUXADCSWTROL signal is from SW or HW** 1'b0: HW mode 1'b1: SW mode

1C02 **ACCDET_CON1** **ACCDET Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										accdet_anaswctrl_sel			ACCDET_EINT_SEQ_INIT	ACCDET_EINTDET_EN	ACCDET_SEQ_INIT	ACCDET_EN
Type										RW			RW	RW	RW	RW
Reset										0			0	0	0	0

Bit(s)	Name	Description
6	accdet_anaswctrl_se	**Selects who controls the connection between auxadc and accdet**

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Bit(s)	Name	Description
	l	**when in hook-key status** 1'b0: auxadc 1'b1: accdet
3	ACCDET_EINT_SEQ_INIT	**Initializes EINT status default value** 1'b0: Disable 1'b1: Enable
2	ACCDET_EINTDET_EN	**Enables EINT detection** 1'b0: Disable 1'b1: Enable
1	ACCDET_SEQ_INIT	**Initializes ACCDET status default value** 1'b0: Normal mode 1'b1: Initialized mode
0	ACCDET_EN	**Enables ACCDET** Must be set to 0 before switching to TV mode. 1'b0: Disable 1'b1: Enable

1C04 **ACCDET_CON2** **ACCDET Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACCDET_EINT_PWM_EN	ACCDET_MBIAS_PWM_EN	ACCDET_VTH_PWM_EN	ACCDET_CMP_PWM_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	ACCDET_EINT_PWM_EN	**Enables PWM of ACCDET EINT unit** Disabled in TV mode. 1'b0: Disable 1'b1: Enable
2	ACCDET_MBIAS_PWM_EN	**Enables PWM of ACCDET MBIAS unit** Disabled in TV mode. 1'b0: Disable 1'b1: Enable
1	ACCDET_VTH_PWM_EN	**Enables PWM of ACCDET voltage threshold unit** Disabled in TV mode. 1'b0: Disable 1'b1: Enable
0	ACCDET_CMP_PWM_EN	**Enables PWM of ACCDET comparator** 1'b0: Disable 1'b1: Enable

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1C06 **ACCDET_CON3** **ACCDET Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_WIDTH	**ACCDET PWM width** PWM output frequency = 32,768/(PWM_WIDTH+1)Hz

1C08 **ACCDET_CON4** **ACCDET Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_THRESH	**ACCDET PWM threshold** PWM output duty cycle = (PWM_THRESH+1)/(PWM_WIDTH+1) PWM output high time = (PWM_THRESH+1)/32,768 sec

1C0A **ACCDET_CON5** **ACCDET Control Register 5** **0101**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_FALL_DELAY	ACCDET_RISE_DELAY														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	ACCDET_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET is disabled, the suitable falling delay cycle is necessary.
14:0	ACCDET_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET is enabled, the suitable rising delay cycle is necessary.

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1C0C **ACCDET_CON6** **ACCDET Control Register 6** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE0	**De-bounce time control of state 0** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768Hz in MIC mode.

1C0E **ACCDET_CON7** **ACCDET Control Register 7** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE1	**De-bounce time control of state 1** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768Hz in MIC mode.

1C10 **ACCDET_CON8** **ACCDET Control Register 8** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE2	**De-bounce time control of state 2** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768Hz in MIC mode.

1C12 **ACCDET_CON9** **ACCDET Control Register 9** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUN	**De-bounce time control of state 3**

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Bit(s)	Name	Description
	CE3	De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768Hz in MIC mode.

1C14 **ACCDET_CON10** **ACCDET Control Register 10** **0005**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE4	De-bounce time to control AUXADC when in state 0

1C18 **ACCDET_CON12** **ACCDET Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_IRQ_POLARITY					ACCDET_EINT_IRQ_CLR		ACCDET_IRQ_CLR						ACCDET_EINT_IRQ		ACCDET_IRQ
Type	RW					RW		RW						RO		RO
Reset	0					0		0						0		0

Bit(s)	Name	Description
15	ACCDET_EINT_IRQ_POLARITY	**ACCDET EINT IRQ POLARITY** 1'b0: Falling edge 1'b1: Rising edge
10	ACCDET_EINT_IRQ_CLR	**Clears ACCDET_EINT interrupt status. When ACCDET_EINT interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.**
8	ACCDET_IRQ_CLR	**Clears ACCDET interrupt status** When ACCDET interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET design until both the interrupt status and IRQ_CLR are cleared.
2	ACCDET_EINT_IRQ	**Monitor signal: accdet_eint irq**
0	ACCDET_IRQ	**Monitor signal: accdet irq**

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1C1C	ACCDET_CON14	ACCDET Control Register 14	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_AUDACCDETAUXADCSWCTRL	ACCDET_CMP_CLK	ACCDET_VTH_CLK	ACCDET_MBIAS_CLK												
Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	DA_AUDACCDETAUXADCSWCTRL	Monitor signal: ACCDET to AUXADC switch control
14	ACCDET_CMP_CLK	Monitor signal: Comparator turn on control for accessory detection
13	ACCDET_VTH_CLK	Monitor signal: Threshold voltage turn on for accessory detection
12	ACCDET_MBIAS_CLK	Monitor signal: Earphone bias voltage turn on for accessory detection

1C1E	ACCDET_CON15	ACCDET Control Register 15	0071

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT_PWM_WIDTH			ACCDET_EINT_PWM_THRESH				ACCDET_EINT_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	1	0			

Bit(s)	Name	Description
13:12	ACCDET_EINT_PWM_WIDTH	**ACCDET EINT PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT_PWM_THRESH	**ACCDET EINT PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:3	ACCDET_EINT_DEBOUNCE	**ACCDET EINT debounce time** 4'd0: 0ms (bypass) 4'd1: 0.12ms 4'd2: 0.25ms 4'd3: 0.5ms 4'd4: 0.75ms 4'd5: 1ms

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Bit(s)	Name	Description
		4'd6: 2ms 4'd7: 4ms 4'd8: 8ms 4'd9: 16ms 4'd10: 32ms 4'd11: 48ms 4'd12: 64ms 4'd13: 128ms 4'd14: 256ms 4'd15: 512ms

1C20 **ACCDET_CON16** **ACCDET Control Register 16** **0160**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_PWM_RISE_DELAY										ACCDET_EINT_PWM_FALL_DELAY					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	1	0	1	1					

Bit(s)	Name	Description
15:6	ACCDET_EINT_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT is disabled, the suitable falling delay cycle is necessary.

1C24 **ACCDET_CON18** **ACCDET Control Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_NI_EINTCMPEN	AD_EINTCMPOUT														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_NI_EINTCMPEN	Monitor signal: DA_NI_EINTCMPEN
14	AD_EINTCMPOUT	Monitor signal: AD_EINTCMPOUT

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1E18 **OTP_CON12** **OTP Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_SW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_SW	Current SW trigger read value (de-featured)

1E1A **OTP_CON13** **OTP Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_OTP_RD_ACK		RG_OTP_RD_BUSY
Type														RO		RO
Reset														0		0

Bit(s)	Name	Description
2	RG_OTP_RD_ACK	OTP read ack
0	RG_OTP_RD_BUSY	OTP busy status

1E1C **OTP_CON14** **OTP Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_OTP_PA_SW						
Type										RO						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_OTP_PA_SW	Current SW trigger read row (de-featured)

1E1E **OTP_DOUT_0_15** **OTP dout 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_0_15	

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1E20 **OTP_DOUT_16_31** **OTP dout 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_16_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_16_31	

1E22 **OTP_DOUT_32_47** **OTP dout 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_32_47															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_32_47	

1E24 **OTP_DOUT_48_63** **OTP dout 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_48_63															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_48_63	

1E26 **OTP_DOUT_64_79** **OTP dout 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_64_79															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_64_79	

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1E28 **OTP_DOUT_80_95** **OTP dout 80 95** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_80_95															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_80_95	

1E2A **OTP_DOUT_96_111** **OTP dout 96 111** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_96_111															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_96_111	

1E2C **OTP_DOUT_112_127** **OTP dout 112 127** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_112_127															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_112_127	

1E2E **OTP_DOUT_128_143** **OTP dout 128 143** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_128_143															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_128_143	

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1E30 **OTP_DOUT_144_159** **OTP dout 144 159** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_144_159															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_144_159	

1E32 **OTP_DOUT_160_175** **OTP dout 160 175** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_160_175															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_160_175	

1E34 **OTP_DOUT_176_191** **OTP dout 176 191** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_176_191															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_176_191	

1E36 **OTP_DOUT_192_207** **OTP dout 192 207** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_192_207															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_192_207	

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1E38	OTP_DOUT_208_223	OTP dout 208 223	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_208_223															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_208_223	

1E3A	OTP_DOUT_224_239	OTP dout 224 239	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_224_239															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_224_239	

1E3C	OTP_DOUT_240_255	OTP dout 240 255	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_240_255															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_240_255	

1E3E	OTP_DOUT_256_271	OTP dout 256 271	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_256_271															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_256_271	

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1E40 OTP_DOUT_272_287 OTP dout 272 287 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_272_287															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_272_287	

1E42 OTP_DOUT_288_303 OTP dout 288 303 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_288_303															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_288_303	

1E44 OTP_DOUT_304_319 OTP dout 304 319 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_304_319															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_304_319	

1E46 OTP_DOUT_320_335 OTP dout 320 335 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_320_335															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_320_335	

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1E48 **OTP_DOUT_336_351** **OTP dout 336 351** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_336_351															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_336_351	

1E4A **OTP_DOUT_352_367** **OTP dout 352 367** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_352_367															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_352_367	

1E4C **OTP_DOUT_368_383** **OTP dout 368 383** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_368_383															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_368_383	

1E4E **OTP_DOUT_384_399** **OTP dout 384 399** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_384_399															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_384_399	

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1E50 **OTP_DOUT_400_415** **OTP dout 400 415** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_400_415															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_400_415	

1E52 **OTP_DOUT_416_431** **OTP dout 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_416_431															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_416_431	

1E54 **OTP_DOUT_432_447** **OTP dout 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_432_447															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_432_447	

1E56 **OTP_DOUT_448_463** **OTP dout 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_448_463															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_448_463	

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1E58 OTP_DOUT_464_479 OTP dout 464 479 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_464_479															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_464_479	

1E5A OTP_DOUT_480_495 OTP dout 480 495 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_480_495															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_480_495	

1E5C OTP_DOUT_496_511 OTP dout 496 511 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_496_511															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_496_511	

1E5E OTP_DOUT_512_527 OTP dout 512 527 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_512_527															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_512_527	

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1E60 **OTP_DOUT_528_543** **OTP dout 528 543** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_528_543															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_528_543	

1E62 **OTP_DOUT_544_559** **OTP dout 544 559** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_544_559															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_544_559	

1E64 **OTP_DOUT_560_575** **OTP dout 560 575** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_560_575															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_560_575	

1E66 **OTP_DOUT_576_591** **OTP dout 576 591** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_576_591															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_576_591	

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1E68 **OTP_DOUT_592_607** **OTP dout 592 607** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_592_607															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_592_607	

1E6A **OTP_DOUT_608_623** **OTP dout 608 623** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_608_623															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_608_623	

1E6C **OTP_DOUT_624_639** **OTP dout 624 639** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_624_639															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_624_639	

1E6E **OTP_DOUT_640_655** **OTP dout 640 655** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_640_655															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_640_655	

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1E70 OTP_DOUT_656_671 OTP dout 656 671 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_656_671															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_656_671	

1E72 OTP_DOUT_672_687 OTP dout 672 687 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_672_687															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_672_687	

1E74 OTP_DOUT_688_703 OTP dout 688 703 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_688_703															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_688_703	

1E76 OTP_DOUT_704_719 OTP dout 704 719 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_704_719															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_704_719	

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1E78 **OTP_DOUT_720_735** **OTP dout 720 735** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_720_735															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_720_735	

1E7A **OTP_DOUT_736_751** **OTP dout 736 751** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_736_751															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_736_751	

1E7C **OTP_DOUT_752_767** **OTP dout 752 767** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_752_767															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_752_767	

1E7E **OTP_DOUT_768_783** **OTP dout 768 783** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_768_783															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_768_783	

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1E80 **OTP_DOUT_784_799** **OTP dout 784 799** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_784_799															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_784_799	

1E82 **OTP_DOUT_800_815** **OTP dout 800 815** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_800_815															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_800_815	

1E84 **OTP_DOUT_816_831** **OTP dout 816 831** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_816_831															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_816_831	

1E86 **OTP_DOUT_832_847** **OTP dout 832 847** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_832_847															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_832_847	

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1E88 OTP_DOUT_848_863 OTP dout 848 863 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_848_863															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_848_863	

1E8A OTP_DOUT_864_879 OTP dout 864 879 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_864_879															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_864_879	

1E8C OTP_DOUT_880_895 OTP dout 880 895 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_880_895															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_880_895	

1E8E OTP_DOUT_896_911 OTP dout 896 911 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_896_911															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_896_911	

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1E90	OTP_DOUT_912_927	OTP dout 912 927	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_912_927															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_912_927	

1E92	OTP_DOUT_928_943	OTP dout 928 943	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_928_943															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_928_943	

1E94	OTP_DOUT_944_959	OTP dout 944 959	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_944_959															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_944_959	

1E96	OTP_DOUT_960_975	OTP dout 960 975	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_960_975															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_960_975	

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1E98	OTP_DOUT_976_991	OTP dout 976 991	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_976_991															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_976_991	

1E9A	OTP_DOUT_992_1007	OTP dout 992 1007	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_992_1007															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_992_1007	

1E9C	OTP_DOUT_1008_1023	OTP dout 1008 1023	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1008_1023															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1008_1023	

1E9E	OTP_DOUT_1024_1039	OTP dout 1024 1039	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1024_1039															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1024_1039	

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1EA0 **OTP_DOUT_1040_1055** **OTP dout 1040 1055** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1040_1055															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1040_1055	

1EA2 **OTP_DOUT_1056_1071** **OTP dout 1056 1071** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1056_1071															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1056_1071	

1EA4 **OTP_DOUT_1072_1087** **OTP dout 1072 1087** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1072_1087															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1072_1087	

1EA6 **OTP_DOUT_1088_1103** **OTP dout 1088 1103** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1088_1103															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1088_1103	

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1EA8 OTP_DOUT_1104_1119 OTP dout 1104 1119 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1104_1119															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1104_1119	

1EAA OTP_DOUT_1120_1135 OTP dout 1120 1135 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1120_1135															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1120_1135	

1EAC OTP_DOUT_1136_1151 OTP dout 1136 1151 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1136_1151															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1136_1151	

1EAE OTP_DOUT_1152_1167 OTP dout 1152 1167 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1152_1167															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1152_1167	

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1EB0 **OTP_DOUT_1168_1183** **OTP dout 1168 1183** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1168_1183															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1168_1183	

1EB2 **OTP_DOUT_1184_1199** **OTP dout 1184 1199** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1184_1199															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1184_1199	

1EB4 **OTP_DOUT_1200_1215** **OTP dout 1200 1215** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1200_1215															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1200_1215	

1EB6 **OTP_DOUT_1216_1231** **OTP dout 1216 1231** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1216_1231															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1216_1231	

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1EB8 **OTP_DOUT_1232_1247** **OTP dout 1232 1247** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1232_1247															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1232_1247	

1EBA **OTP_DOUT_1248_1263** **OTP dout 1248 1263** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1248_1263															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1248_1263	

1EBC **OTP_DOUT_1264_1279** **OTP dout 1264 1279** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1264_1279															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1264_1279	

1EBE **OTP_DOUT_1280_1295** **OTP dout 1280 1295** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1280_1295															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1280_1295	

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1EC0	OTP_DOUT_1296_1311	OTP dout 1296 1311	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1296_1311															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1296_1311	

1EC2	OTP_DOUT_1312_1327	OTP dout 1312 1327	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1312_1327															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1312_1327	

1EC4	OTP_DOUT_1328_1343	OTP dout 1328 1343	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1328_1343															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1328_1343	

1EC6	OTP_DOUT_1344_1359	OTP dout 1344 1359	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1344_1359															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1344_1359	

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1EC8	OTP_DOUT_1360_1375	OTP dout 1360 1375	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1360_1375															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1360_1375	

1ECA	OTP_DOUT_1376_1391	OTP dout 1376 1391	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1376_1391															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1376_1391	

1ECC	OTP_DOUT_1392_1407	OTP dout 1392 1407	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1392_1407															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1392_1407	

1ECE	OTP_DOUT_1408_1423	OTP dout 1408 1423	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1408_1423															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1408_1423	

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1ED0 **OTP_DOUT_1424_1439** **OTP dout 1424 1439** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1424_1439															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1424_1439	

1ED2 **OTP_DOUT_1440_1455** **OTP dout 1440 1455** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1440_1455															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1440_1455	

1ED4 **OTP_DOUT_1456_1471** **OTP dout 1456 1471** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1456_1471															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1456_1471	

1ED6 **OTP_DOUT_1472_1487** **OTP dout 1472 1487** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1472_1487															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1472_1487	

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1ED8 **OTP_DOUT_1488_1503** **OTP dout 1488 1503** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1488_1503															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1488_1503	

1EDA **OTP_DOUT_1504_1519** **OTP dout 1504 1519** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1504_1519															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1504_1519	

1EDC **OTP_DOUT_1520_1535** **OTP dout 1520 1535** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_1520_1535															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_1520_1535	

200C **DCXO_CW04** **DCXO Code Word 4** **FF55**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CDAC_LPM								XO_CDAC_FPM							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15:8	XO_CDAC_LPM	XO CDAC code (complement) during LPM
7:0	XO_CDAC_FPM	XO CDAC code (complement) during FPM

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200E **DCXO_CW05** **DCXO Code Word 5** **DD40**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_FPM															
Type	RW															
Reset	1	1														

Bit(s)	Name	Description
15:14	XO_COFST_FPM	XO CDAC offset code during FPM

2010 **DCXO_CW06** **DCXO Code Word 6** **2318**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_LPM															
Type	RW															
Reset	0	0														

Bit(s)	Name	Description
15:14	XO_COFST_LPM	XO CDAC offset code during LPM

2026 **DCXO_CW15** **DCXO Code Word 15** **A2AA**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_EXTBUF7_HD		RG_XO_EXTBUF6_HD				RG_XO_EXTBUF4_HD		RG_XO_EXTBUF3_HD		RG_XO_EXTBUF2_HD		RG_XO_EXTBUF1_HD			
Type	RW		RW				RW		RW		RW		RW			
Reset	1	0	1	0			1	0	1	0	1	0	1	0		

Bit(s)	Name	Description
15:14	RG_XO_EXTBUF7_HD	XO control signal of EXTBUF7 output driving strength
13:12	RG_XO_EXTBUF6_HD	XO control signal of EXTBUF6 output driving strength
9:8	RG_XO_EXTBUF4_HD	XO control signal of EXTBUF4 output driving strength
7:6	RG_XO_EXTBUF3_HD	XO control signal of EXTBUF3 output driving strength
5:4	RG_XO_EXTBUF2_HD	XO control signal of EXTBUF2 output driving strength
3:2	RG_XO_EXTBUF1_HD	XO control signal of EXTBUF1 output driving strength

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2028 **DCXO_CW16** **DCXO Code Word 16** **A8AA**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			XO_EXTBUF7_ISET_M		XO_EXTBUF6_ISET_M				XO_EXTBUF4_ISET_M		XO_EXTBUF3_ISET_M		XO_EXTBUF2_ISET_M		XO_EXTBUF1_ISET_M	
Type			RW		RW				RW		RW		RW		RW	
Reset			1	0	1	0			1	0	1	0	1	0	1	0

Bit(s)	Name	Description
13:12	XO_EXTBUF7_ISET_M	XO control signal of current on EXTBUF7
11:10	XO_EXTBUF6_ISET_M	XO control signal of current on EXTBUF6
7:6	XO_EXTBUF4_ISET_M	XO control signal of current on EXTBUF4
5:4	XO_EXTBUF3_ISET_M	XO control signal of current on EXTBUF3
3:2	XO_EXTBUF2_ISET_M	XO control signal of current on EXTBUF2
1:0	XO_EXTBUF1_ISET_M	XO control signal of current on EXTBUF1

202C **DCXO_CW18** **DCXO Code Word 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AUXOUT_SEL										XO_STATIC_AUXOUT_SEL					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:6	XO_AUXOUT_SEL	Selects dynamic AuxOut
5:0	XO_STATIC_AUXOUT_SEL	Selects static AuxOut

202E **DCXO_CW19** **DCXO Code Word 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_STATIC_AUXOUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XO_STATIC_AUXOUT	Static Auxout readout

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2200 **CHR_CON0** **Charger Control Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VCDT_HV_DET	RGS_VCDT_LV_DET	RGS_CHRDET					
Type									RO	RO	RO					
Reset									0	0	0					

Bit(s)	Name	Description
7	RGS_VCDT_HV_DET	**Charger-in high voltage detection (with de-bounce)** 0: Charge-in voltage < VCDT_HV_VTH 1: Charge-in voltage > VCDT_HV_VTH
6	RGS_VCDT_LV_DET	**Charger-in low voltage detection (with de-bounce)** 0: Charge-in voltage < VCDT_LV_VTH 1: Charge-in voltage > VCDT_LV_VTH
5	RGS_CHRDET	**Detects charger-in** 0: No valid charger detected 1: Valid charger detected

2202 **CHR_CON1** **Charger Control Register 1** **00C2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCDT_HV_VTH				RG_VCDT_LV_VTH			
Type									RW				RW			
Reset									1	1	0	0	0	0	1	0

Bit(s)	Name	Description
7:4	RG_VCDT_HV_VTH	**1111: 14.0V** 1110: 12.5V 1101: 11.5V 1100: 10.5V (RG_VCDT_HV_VTH default) 1011: 9.5V 1010: 8.5V 1001: 7.5V 1000: 7.0V 0111: 6.5V 0110: 6.0V 0101: 4.45V 0100: 4.4V 0011: 4.35V 0010: 4.3V (RG_VCDT_LV_VTH default) 0001: 4.25V 0000: 4.2V
3:0	RG_VCDT_LV_VTH	**1111: 14.0V** 1110: 12.5V 1101: 11.5V 1100: 10.5V (RG_VCDT_HV_VTH default) 1011: 9.5V 1010: 8.5V 1001: 7.5V 1000: 7.0V 0111: 6.5V 0110: 6.0V

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Bit(s)	Name	Description
		0101: 4.45V 0100: 4.4V 0011: 4.35V 0010: 4.3V (RG_VCDT_LV_VTH default) 0001: 4.25V 0000: 4.2V

220A CHR_CON5 Charger Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ENVTEM_EN	RG_ENVTEM_D
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_ENVTEM_EN	**Blocks CHR_DET signal to start_up** 0: N/A 1: Enable write
0	RG_ENVTEM_D	**Blocks CHR_DET signal to start_up** 1: Block 0: Not block

220E CHR_CON7 Charger Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_ADCIN_CHR_EN	RG_ADCIN_VSEN_EN	RG_ADCIN_VBAT_EN	RG_ADCIN_VSEN_EXT_BATON_EN	RG_ADCIN_VSEN_MUX_EN								
Type				RW	RW	RW	RW	RW								
Reset				0	0	0	0	0								

Bit(s)	Name	Description
12	RG_ADCIN_CHR_EN	**Enables AUXADC input source for CHR** 0: Disable 1: Enable
11	RG_ADCIN_VSEN_EN	**Enables AUXADC input source for VSEN** 0: Disable 1: Enable
10	RG_ADCIN_VBAT_EN	**Enables AUXADC input source for VBAT** 0: Disable 1: Enable
9	RG_ADCIN_VSEN_EXT_BATON_EN	**Enables AUXADC input source for external source to be switched to AUXADC's Ch3**

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Bit(s)	Name	Description
		0: Disable 1: Enable
8	RG_ADCIN_VSEN_MUX_EN	**Enables AUXADC input source for VSEN to be switched to VBAT's divider** 0: Disable 1: Enable

2210 **PCHR_VREF_ANA_DA0** **PCHR_VREF DA Register 0** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BATON_TDET_EN		DA_QI_BATON_LT_EN
Type														RW		RW
Reset														0		1

Bit(s)	Name	Description
2	BATON_TDET_EN	0: N/A 1: Enable BATON temperature detection
0	DA_QI_BATON_LT_EN	

2214 **PCHR_VREF_ANA_CON1** **PCHR_VREF Control Register 1** **2018**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_OTG_BVALID_EN	RG_HW_VTH_CTRL	RG_HW_VTH2		RG_HW_VTH1					RG_BATON_EN				
Type			RW	RW	RW		RW					RW				
Reset			1	0	0	0	0	0				1				

Bit(s)	Name	Description
13	RG_OTG_BVALID_EN	**Enables OTG BValid detection** 1: Enable 0: Disable
12	RG_HW_VTH_CTRL	**Selects BATON low temperature threshold 1, 2**
11:10	RG_HW_VTH2	**Selects BATON low temperature threshold 2**
9:8	RG_HW_VTH1	**Selects BATON low temperature threshold 1**
4	RG_BATON_EN	**Enables BATON battery detection comparator** 0: Disable 1: Enable (default)

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2216 **PCHR_VREF_ANA_CON2** **PCHR_VREF Control Register 2** **00C2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_LBAT_INT_VTH										
Type						RW										
Reset						0	0	0	1	1						

Bit(s)	Name	Description
10:6	RG_LBAT_INT_VTH	**LBAT_INT threshold voltage** 00000: 2.5V 00001: 2.55V 00010: 2.6V 00011: 2.65V (default) 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V 01001: 2.95V 01010: 3.0V 01011: 3.05V 01100: 3.1V 01101: 3.15V 01110: 3.2V 01111: 3.25V 10000: 3.3V 10001: 3.35V 10010: 3.4V

2218 **PCHR_VREF_ANA_CON3** **PCHR_VREF Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCDT_UVLO_VTH					RGS_BATON_HV	RGS_CHR_LDO_DET	RGS_OTG_BVALID_DET	RGS_BATON_UNDET				
Type				RW					RO	RO	RO	RO				
Reset				0	0	0	0		0	0	0	0				

Bit(s)	Name	Description
12:9	RG_VCDT_UVLO_VTH	**UV_falling:** 3.9V, default (+/-6%, include resistor 1%) 2.8~3.9 per 0.1V/Step, (+/-6%, include resistor 1%) Add for fast charging (LVHI).
7	RGS_BATON_HV	**BATON HV detect flag**
6	RGS_CHR_LDO_DET	**Charger LDO detection** 1: Detected 0: Not detected
5	RGS_OTG_BVALID_DET	**OTG BValid detected** 1: Detected

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Bit(s)	Name	Description
		0: Not detected
4	RGS_BATON_UNDET	**Battery-on undetected** 1: Not detected 0: Detected

2400 GPIO_DIR0 GPIO Direction Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_DIR0													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	GPIO_DIR0	**GPIO direction control** 1'b0: Input 1'b1: Output

2402 GPIO_DIR0_SET GPIO_DIR0 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_DIR0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_DIR0_SET	**Sets up GPIO_DIR0** 1'b0: Not set 1'b1: Set

2404 GPIO_DIR0_CLR GPIO_DIR0 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_DIR0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_DIR0_CLR	**Clears GPIO_DIR0** 1'b0: Not clear 1'b1: Clear

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2406 **GPIO_PULLEN0** **GPIO Pull-up/Pull-down Enable Register 0** **0CE7**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_PULLEN0													
Type			RW													
Reset			0	0	1	1	0	0	1	1	1	0	0	1	1	1

Bit(s)	Name	Description
13:0	GPIO_PULLEN0	**Enables GPIO pull-up/pull-down** 1'b0: Disable 1'b1: Enable

2408 **GPIO_PULLEN0_SET** **GPIO_PULLEN0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_PULLEN0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_PULLEN0_SET	**Sets up GPIO_PULLEN0** 1'b0: Not set 1'b1: Set

240A **GPIO_PULLEN0_CLR** **GPIO_PULLEN0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_PULLEN0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_PULLEN0_CLR	**Clears GPIO_PULLEN0** 1'b0: Not clear 1'b1: Clear

240C **GPIO_PULLSEL0** **GPIO Pull-up/Pull-down Selection Register 0** **0087**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_PULLSEL0													
Type			RW													
Reset			0	0	0	0	0	0	1	0	0	0	0	1	1	1

Bit(s)	Name	Description
13:0	GPIO_PULLSEL0	**Selects GPIO pull-up/pull-down**

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Bit(s)	Name	Description
		1'b0: Pull-down 1'b1: Pull-up

240E GPIO_PULLSEL0_SET GPIO_PULLSEL0 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_PULLSEL0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_PULLSEL0_SET	**Sets up GPIO_PULLSEL0** 1'b0: Not set 1'b1: Set

2410 GPIO_PULLSEL0_CLR GPIO_PULLSEL0 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_PULLSEL0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_PULLSEL0_CLR	**Clears GPIO_PULLSEL0** 1'b0: Not clear 1'b1: Clear

2412 GPIO_DINV0 GPIO Data Inversion Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_DINV0													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	GPIO_DINV0	**GPIO inversion control** 1'b0: Disable 1'b1: Enable

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2414 GPIO_DINV0_SET **GPIO_DINV0 Register SET** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_DINV0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_DINV0_SET	**Sets up GPIO_DINV0** 1'b0: Not set 1'b1: Set

2416 GPIO_DINV0_CLR **GPIO_DINV0 Register CLR** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_DINV0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_DINV0_CLR	**Clears GPIO_DINV0** 1'b0: Not clear 1'b1: Clear

2418 GPIO_DOUT0 **GPIO Data Output Register 0** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_DOUT0													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	GPIO_DOUT0	**GPIO data output value** 1'b0: Output 0 1'b1: Output 1

241A GPIO_DOUT0_SET **GPIO_DOUT0 Register SET** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_DOUT0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_DOUT0_SET	**Sets up GPIO_DOUT0**

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Bit(s)	Name	Description
		1'b0: Not set 1'b1: Set

241C GPIO_DOUT0_CLR GPIO_DOUT0 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_DOUT0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_DOUT0_CLR	**Clears GPIO_DOUT0** 1'b0: Not clear 1'b1: Clear

241E GPIO_PI0 GPIO Data Input Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_PI0													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	GPIO_PI0	GPIO data input value

2420 GPIO_POE0 GPIO Data Direction Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			GPIO_POE0													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	GPIO_POE0	GPIO direction value

2422 GPIO_MODE0 GPIO Mode Control Register 0 1249

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO4_MODE			GPIO3_MODE			GPIO2_MODE			GPIO1_MODE			GPIO0_MODE		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Name	Description
14:12	GPIO4_MODE	**GPIO 4 Mode Selection**

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Bit(s)	Name	Description
		0: GPIO4 (IO) 1: RTC_32K1V8_1 (O) 2: INT_1 (O) 3: Reserved 4: Reserved 5: Reserved 6: TEST_IN3 (I) 7: TEST_OUT3 (O)
11:9	GPIO3_MODE	**Selects GPIO 3 mode** 0: GPIO3 (IO) 1: RTC_32K1V8_0 (O) 2: Reserved 3: Reserved 4: Reserved 5: TEST_CK2 (I) 6: TEST_IN2 (I) 7: TEST_OUT2 (O)
8:6	GPIO2_MODE	**Selects GPIO 2 mode** 0: GPIO2 (IO) 1: SRCLKEN_IN1 (I) 2: Reserved 3: Reserved 4: Reserved 5: TEST_CK1 (I) 6: TEST_IN1 (I) 7: TEST_OUT1 (O)
5:3	GPIO1_MODE	**Selects GPIO 1 mode** 0: GPIO1 (IO) 1: SRCLKEN_IN0 (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: TEST_IN0 (I) 7: TEST_OUT0 (O)
2:0	GPIO0_MODE	**Selects GPIO 0 mode** 0: GPIO0 (IO) 1: HOMEKEY (I) 2: INT_0 (O) 3: Reserved 4: Reserved 5: TEST_CK0 (I) 6: Reserved 7: Reserved

2424 GPIO_MODE0_SET **GPIO_MODE0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_MODE0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_MODE0_SET	**Sets up GPIO_MODE0**

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Bit(s)	Name	Description
		1'b0: Not set 1'b1: Set

2426 **GPIO_MODE0_CLR** **GPIO_MODE0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_MODE0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_MODE0_CLR	**Clears GPIO_MODE0** 1'b0: Not clear 1'b1: Clear

2428 **GPIO_MODE1** **GPIO Mode Control Register 1** **1249**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO9_MODE			GPIO8_MODE			GPIO7_MODE			GPIO6_MODE			GPIO5_MODE		
Type		RW			RW			RW			RW			RW		
Reset		0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Name	Description
14:12	GPIO9_MODE	**Selects GPIO 9 mode** 0: GPIO9 (IO) 1: SPI_MISO (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
11:9	GPIO8_MODE	**Selects GPIO 8 mode** 0: GPIO8 (IO) 1: SPI_MOSI (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	GPIO7_MODE	**Selects GPIO 7 mode** 0: GPIO7 (IO) 1: SPI_CSN (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

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Bit(s)	Name	Description
5:3	GPIO6_MODE	**Selects GPIO 6 mode** 0: GPIO6 (IO) 1: SPI_CLK (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
2:0	GPIO5_MODE	**Selects GPIO 5 mode** 0: GPIO5 (IO) 1: SCP_VREQ_VAO (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: TEST_IN4 (I) 7: TEST_OUT4 (O)

242A **GPIO_MODE1_SET** **GPIO_MODE1 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_MODE1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_MODE1_SET	**Sets up GPIO_MODE1** 1'b0: Not set 1'b1: Set

242C **GPIO_MODE1_CLR** **GPIO_MODE1 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_MODE1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_MODE1_CLR	**Clears GPIO_MODE1** 1'b0: Not clear 1'b1: Clear

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242E **GPIO_MODE2** **GPIO Mode Control Register 2** **0249**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO13_MODE			GPIO12_MODE			GPIO11_MODE			GPIO10_MODE		
Type					RW			RW			RW			RW		
Reset					0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Name	Description
11:9	GPIO13_MODE	**Selects GPIO 13 mode** 0: GPIO13 (IO) 1: VOW_CLK_MISO (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
8:6	GPIO12_MODE	**Selects GPIO 12 mode** 0: GPIO12 (IO) 1: AUD_DAT_MISO (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: TEST_IN7(I) 7: TEST_OUT7(O)
5:3	GPIO11_MODE	**Selects GPIO 11 mode** 0: GPIO11 (IO) 1: AUD_DAT_MOSI (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: TEST_IN6(I) 7: TEST_OUT6(O)
2:0	GPIO10_MODE	**Selects GPIO 10 mode** 0: GPIO10 (IO) 1: AUD_CLK (I) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: TEST_IN5 (I) 7: TEST_OUT5 (O)

2430 **GPIO_MODE2_SET** **GPIO_MODE2 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_MODE2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	GPIO_MODE2_SET	**Sets up GPIO_MODE2** 1'b0: Not set 1'b1: Set

2432 **GPIO_MODE2_CLR** **GPIO_MODE2 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_MODE2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_MODE2_CLR	**Clears GPIO_MODE2** 1'b0: Not clear 1'b1: Clear

2434 **GPIO_RSV** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_RSV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GPIO_RSV	

2E00 **BIF_CON0** **BIF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_0										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_0	Command queue 0

2E02 **BIF_CON1** **BIF Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_1										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
10:0	BIF_COMMAND_1	Command queue 1

2E04 BIF_CON2 BIF Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_2										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_2	Command queue 2

2E06 BIF_CON3 BIF Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_3										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_3	Command queue 3

2E08 BIF_CON4 BIF Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_4										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_4	Command queue 4

2E0A BIF_CON5 BIF Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_5										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_5	**Command queue 5**

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2E0C **BIF_CON6** **BIF Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_6										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_6	Command queue 6

2E0E **BIF_CON7** **BIF Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_7										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_7	Command queue 7

2E10 **BIF_CON8** **BIF Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_8										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_8	Command queue 8

2E12 **BIF_CON9** **BIF Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_9										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_9	Command queue 9

2E14 **BIF_CON10** **BIF Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_10										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
10:0	BIF_COMMAND_10	Command queue 10

2E16 BIF_CON11 BIF Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_11										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_11	Command queue 11

2E18 BIF_CON12 BIF Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_12										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_12	Command queue 12

2E1A BIF_CON13 BIF Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_13										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_13	Command queue 13

2E1C BIF_CON14 BIF Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						BIF_COMMAND_14										
Type						RW										
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:0	BIF_COMMAND_14	Command queue 14

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2E1E BIF_CON15 BIF Control Register 15 4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_TRASFER_NUM						BIF_COMMAND_TYPE									
Type	RW						RW									
Reset	0	1	0	0			0	0								

Bit(s)	Name	Description
15:12	BIF_TRASFER_NUM	**Total transfer number in command que**
9:8	BIF_COMMAND_TYPE	**Command type** 2'b00: Write 2'b01: Read data 2'b10: Read response

2E20 BIF_CON16 BIF Control Register 16 1431

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_STOP_SET							BIF_LOGIC_1_SET					BIF_LOGIC_0_SET			
Type	RW							RW					RW			
Reset	0	0	0	1	0	1		0	0	0	1	1	0	0	0	1

Bit(s)	Name	Description
15:10	BIF_STOP_SET	**Sets up stop signal spec** 6'd0: 0T 6'd1: 1T 6'd2: 2T 6'dN: NT
8:4	BIF_LOGIC_1_SET	**Sets up logic "1" period spec** 5'd0: 0T 5'd1: 1T 5'd2: 2T 5'dN: NT
3:0	BIF_LOGIC_0_SET	**Sets up logic "0" period spec** 4'd0: 0T 4'd1: 1T 4'd2: 2T 4'dN: NT

2E22 BIF_CON17 BIF Control Register 17 1010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_READ_EXPECT_NUM											BIF_DEBOUNCE_EN				
Type	RW											RW				
Reset	0	0	0	1								1				

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Bit(s)	Name	Description
15:12	BIF_READ_EXPECT_NUM	**Expects the number of Read back data** 0: 0 1: 1 data package
4	BIF_DEBOUNCE_EN	**Enables debounce function** 1'b0: Disable 1'b1: Enable

2E24 BIF_CON18 BIF Control Register 18 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BIF_TRASACT_TRIGGER
Type																RW
Reset																0

Bit(s)	Name	Description
0	BIF_TRASACT_TRIGGER	**Trigger signal** 1'b1: Trigger BIF module

2E26 BIF_CON19 BIF Control Register 19 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BIF_RESPONSE									BIF_DATA_NUM			
Type				RO									RO			
Reset				0									0	0	0	0

Bit(s)	Name	Description
12	BIF_RESPONSE	**Response result** 1'b1: Positive response 1'b0: Negative response
3:0	BIF_DATA_NUM	**Number of Read back data**

2E28 BIF_CON20 BIF Control Register 20 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_0							BIF_ACK_0	BIF_DATA_0							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	BIF_ERROR_0	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_0	
7:0	BIF_DATA_0	**Read back data**

2E2A **BIF_CON21** **BIF Control Register 21** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_1							BIF_ACK_1	BIF_DATA_1							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_1	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_1	
7:0	BIF_DATA_1	**Read back data**

2E2C **BIF_CON22** **BIF Control Register 22** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_2							BIF_ACK_2	BIF_DATA_2							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_2	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_2	
7:0	BIF_DATA_2	**Read back data**

2E2E **BIF_CON23** **BIF Control Register 23** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_3							BIF_ACK_3	BIF_DATA_3							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	BIF_ERROR_3	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_3	
7:0	BIF_DATA_3	**Read back data**

2E30 **BIF_CON24** **BIF Control Register 24** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_4							BIF_ACK_4	BIF_DATA_4							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_4	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_4	
7:0	BIF_DATA_4	**Read back data**

2E32 **BIF_CON25** **BIF Control Register 25** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_5							BIF_ACK_5	BIF_DATA_5							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_5	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_5	
7:0	BIF_DATA_5	**Read back data**

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2E34 BIF_CON26 BIF Control Register 26 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_6							BIF_ACK_6	BIF_DATA_6							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_6	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_6	
7:0	BIF_DATA_6	**Read back data**

2E36 BIF_CON27 BIF Control Register 27 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_7							BIF_ACK_7	BIF_DATA_7							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_7	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_7	
7:0	BIF_DATA_7	**Read back data**

2E38 BIF_CON28 BIF Control Register 28 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_8							BIF_ACK_8	BIF_DATA_8							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_8	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_8	
7:0	BIF_DATA_8	**Read back data**

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2E3A BIF_CON29 BIF Control Register 29 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_ERROR_9							BIF_ACK_9	BIF_DATA_9							
Type	RO							RO	RO							
Reset	0							1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	BIF_ERROR_9	**Error happens or not** 1'b1: Error exists. 1'b0: No error
8	BIF_ACK_9	
7:0	BIF_DATA_9	**Read back data**

2E3E BIF_CON31 BIF Control Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_BUS_STATUS	BIF_TOTAL_VALID	BIF_BAT_UNDET	BIF_TIMEOUT	BIF_IRQ										BIF_IRQ_CLR	BIF_BACK_NORMAL
Type	RO	RO	RO	RO	RO										RW	RW
Reset	0	0	0	0	0										0	0

Bit(s)	Name	Description
15	BIF_BUS_STATUS	**Busy: BIF is still in action** 1'b0: Complete 1'b1: Busy
14	BIF_TOTAL_VALID	**Error happens or not in all read data** 1'b1: Error exists (for all data) 1'b0: No error
13	BIF_BAT_UNDET	**Battery status** 1'b0: Battery exists. 1'b1: Battery undetected
12	BIF_TIMEOUT	**Timeout status** 1'b1: Time out
11	BIF_IRQ	**BIF interrupt status** Because this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design. 1'b1: Interrupt issue
1	BIF_IRQ_CLR	**Clears BIF interrupt status** When BIF interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status.
0	BIF_BACK_NORMAL	**Finishes interrupt mode** 1'b1: Abort interrupt mode

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2E40 BIF_CON32 BIF Control Register 32 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_POWER_UP											BIF_POWER_UP_COUNT				
Type	RW											RW				
Reset	0											1	0	0	0	0

Bit(s)	Name	Description
15	BIF_POWER_UP	**Powers up trigger** 1'b1: Power up slave device
4:0	BIF_POWER_UP_COUNT	**Powers up counter setting** 5'd0: 0 5'd1: 1T 5'd2: 2T 5'dN: NT

2E4A BIF_CON37 BIF Control Register 37 000B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_TIMEOUT_SET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
15:0	BIF_TIMEOUT_SET	**Sets up timeout spec** 16'd0: 0T 16'd1: 1T 16'd2: 2T 16'dN: NT

2E4C BIF_CON38 BIF Control Register 38 8022

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIF_RX_DEG_EN						BIF_RX_DEG_WND									
Type	RW						RW									
Reset	1						0	0	0	0	1	0	0	0	1	0

Bit(s)	Name	Description
15	BIF_RX_DEG_EN	**Enables deglitch function** 1'b0: Bypass 1'b1: Enable HW deglitch function
9:0	BIF_RX_DEG_WND	**Filter window** 10'd0: 1T 10'd1: 2T 10'd2: 3T 10'dN: (N+1)T

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300E	FGADC_CUR_CON0	FGADC_CUR Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CURRENT_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CURRENT_OUT	Current output charge of first stage[15:0]

3016	FGADC_CAR_CON0	FGADC_CAR Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_31_16	Current charge value[31:16]

3018	FGADC_CAR_CON1	FGADC_CAR Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_15_00	Current charge value[15:0]

302A	FGADC_NCAR_CON0	FGADC_NCAR Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NCAR_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NCAR_31_16	Current n_charge value[31:16]

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302C **FGADC_NCAR_CON1** **FGADC_NCAR Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NCAR_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NCAR_15_00	Current n_charge value[15:0]

3032 **FGADC_IAVG_CON0** **FGADC_IAVG Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_IAVG_VLD				FG_IAVG_27_16											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	FG_IAVG_VLD	**FGADC average current valid** 1'b0: Invalid 1'b1: Valid
11:0	FG_IAVG_27_16	**Current FGADC average current [27:16]**

3034 **FGADC_IAVG_CON1** **FGADC_IAVG Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_IAVG_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_IAVG_15_00	**Current FGADC average current [15:0]** Unit of FG_IAVG is [LSB of charge / 32]

303E **FGADC_NTER_CON0** **FGADC_NTER Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FG_NTER_29_16													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
13:0	FG_NTER_29_16	Current charge time value[29:16]

3040 **FGADC_NTER_CON1** **FGADC_NTER Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_15_00	Current charge time value[15:0]

3200 **AUXADC_ADC0** **AUXADC ADC Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0	AUXADC_ADC_OUT_CH0														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

3202 **AUXADC_ADC1** **AUXADC ADC Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1	AUXADC_ADC_OUT_CH1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding

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Bit(s)	Name	Description
		1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

3204 **AUXADC_ADC2** **AUXADC ADC Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH2**				**AUXADC_ADC_OUT_CH2**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH2	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

3206 **AUXADC_ADC3** **AUXADC ADC Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH3**				**AUXADC_ADC_OUT_CH3**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

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3208	AUXADC_ADC4	AUXADC ADC Register 4	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

320A	AUXADC_ADC5	AUXADC ADC Register 5	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH5				AUXADC_ADC_OUT_CH5											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

320C	AUXADC_ADC6	AUXADC ADC Register 6	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH6				AUXADC_ADC_OUT_CH6											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

320E **AUXADC_ADC7** **AUXADC ADC Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7	AUXADC_ADC_OUT_CH7														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

3210 **AUXADC_ADC8** **AUXADC ADC Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH8				AUXADC_ADC_OUT_CH8											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

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3212 AUXADC_ADC9 AUXADC ADC Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH9	AUXADC_ADC_OUT_CH9														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

3214 AUXADC_ADC10 AUXADC ADC Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH10				AUXADC_ADC_OUT_CH10											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH10	**AUXADC channel 10 output data**

3216 AUXADC_ADC11 AUXADC ADC Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH11				AUXADC_ADC_OUT_CH11											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready (used for BIF)** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data (used for BIF)**

3218 **AUXADC_ADC12** **AUXADC ADC Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15	AUXADC_ADC_OUT_CH12_15														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

321A **AUXADC_ADC13** **AUXADC ADC Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_THR_HW				AUXADC_ADC_OUT_THR_HW											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_THR_HW	**AUXADC channel 4 output data ready (for pmic_temp)** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_THR_HW	**AUXADC channel 4 output data**

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321C **AUXADC_ADC14** **AUXADC ADC Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT				AUXADC_ADC_OUT_LBAT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

321E **AUXADC_ADC15** **AUXADC ADC Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT2				AUXADC_ADC_OUT_LBAT2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT2	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT2	**AUXADC low battery output data**

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3220	AUXADC_ADC16	AUXADC ADC Register 16	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_GPS	AUXADC_ADC_OUT_CH7_BY_GPS														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_GPS	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_GPS	**AUXADC channel 7 output data**

3222	AUXADC_ADC17	AUXADC ADC Register 17	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_MD	AUXADC_ADC_OUT_CH7_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_MD	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_MD	**AUXADC channel 7 output data**

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3224	AUXADC_ADC18	AUXADC ADC Register 18	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_AP	AUXADC_ADC_OUT_CH7_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_AP	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_AP	**AUXADC channel 7 output data**

3226	AUXADC_ADC19	AUXADC ADC Register 19	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_MD				AUXADC_ADC_OUT_CH4_BY_MD											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_MD	**AUXADC channel 4 output data**

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3228	AUXADC_ADC20	AUXADC ADC Register 20	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_PWRON_PCHR	AUXADC_ADC_OUT_PWRON_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_PWRON_PCHR	**AUXADC power on output data ready (BATADC)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_PWRON_PCHR	**AUXADC power on output data**

322A	AUXADC_ADC21	AUXADC ADC Register 21	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_PWRON_SWCHR	AUXADC_ADC_OUT_PWRON_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_PWRON_SWCHR	**AUXADC power on output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_PWRON_SWCHR	**AUXADC power on output data**

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322C **AUXADC_ADC22** **AUXADC ADC Register 22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready (BATADC)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

322E **AUXADC_ADC23** **AUXADC ADC Register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_SWCHR	AUXADC_ADC_OUT_WAKEUP_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

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3230	AUXADC_ADC24	AUXADC ADC Register 24	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_MD	AUXADC_ADC_OUT_CH0_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_MD	**AUXADC channel output data**

3232	AUXADC_ADC25	AUXADC ADC Register 25	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_AP	AUXADC_ADC_OUT_CH0_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_AP	**AUXADC channel output data**

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3234	AUXADC_ADC26	AUXADC ADC Register 26	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_MD	AUXADC_ADC_OUT_CH1_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_MD	**AUXADC channel output data**

3236	AUXADC_ADC27	AUXADC ADC Register 27	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_AP	AUXADC_ADC_OUT_CH1_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_AP	**AUXADC channel output data**

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3238	AUXADC_ADC28	AUXADC ADC Register 28	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_TEMP				AUXADC_ADC_OUT_BAT_TEMP											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_TEMP	**AUXADC BAT_TEMP output data ready** 0: AUXADC BAT_TEMP data proceeding 1: AUXADC BAT_TEMP data ready
11:0	AUXADC_ADC_OUT_BAT_TEMP	**AUXADC BAT_TEMP output data**

323A	AUXADC_ADC29	AUXADC ADC Register 29	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC_PCHR	AUXADC_ADC_OUT_FGADC_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC_PCHR	**AUXADC output data ready (BATADC)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC_PCHR	**AUXADC output data**

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323C AUXADC_ADC30 AUXADC ADC Register 30 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC_SWCHR	AUXADC_ADC_OUT_FGADC_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC_SWCHR	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC_SWCHR	**AUXADC output data**

323E AUXADC_ADC31 AUXADC ADC Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_PLUGIN_PCHR	AUXADC_ADC_OUT_BAT_PLUGIN_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_PLUGIN_PCHR	**AUXADC output data ready (BATADC)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_BAT_PLUGIN_PCHR	**AUXADC output data**

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3240 AUXADC_ADC32 AUXADC ADC Register 32 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BAT_PLUGIN_SWCHR	AUXADC_ADC_OUT_BAT_PLUGIN_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BAT_PLUGIN_SWCHR	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_BAT_PLUGIN_SWCHR	**AUXADC output data**

3242 AUXADC_ADC33 AUXADC ADC Register 33 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP	AUXADC_ADC_OUT_IMP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP	**AUXADC output data**

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3244 AUXADC_ADC34 AUXADC ADC Register 34 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP_AVG	AUXADC_ADC_OUT_IMP_AVG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP_AVG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP_AVG	**AUXADC output data**

3246 AUXADC_ADC35 AUXADC ADC Register 35 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	AUXADC channel output raw data

3248 AUXADC_ADC36 AUXADC ADC Register 36 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDRT	AUXADC_ADC_OUT_MDRT														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OU	**AUXADC output data**

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Bit(s)	Name	Description
	T_MDRT	

324C **AUXADC_ADC38** **AUXADC ADC Register 38** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_JEITA				AUXADC_ADC_OUT_JEITA											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_JEITA	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_JEITA	**AUXADC output data**

3256 **AUXADC_ADC43** **AUXADC ADC Register 43** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_NAG	AUXADC_ADC_OUT_NAG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_NAG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_NAG	**AUXADC output data**

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3258	AUXADC_ADC44	AUXADC ADC Register 44	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_BATID				AUXADC_ADC_OUT_BATID											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_BATID	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_BATID	**AUXADC output data**

329A	AUXADC_STA0	AUXADC_STA0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_WAKEUP	AUXADC_ADC_BUSY_IN_BAT_TEMP	AUXADC_ADC_BUSY_IN_LBAT2	AUXADC_ADC_BUSY_IN_LBAT	AUXADC_ADC_BUSY_IN											
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 1: BUSY 0: IDLE
14	AUXADC_ADC_BUSY_IN_BAT_TEMP	**ADC busy status** 1: BUSY 0: IDLE
13	AUXADC_ADC_BUSY_IN_LBAT2	**ADC busy status** 1: BUSY 0: IDLE
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 1: BUSY 0: IDLE
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC BUSY STATUS, bit[11] = CH11 ~ bit[0] = CH0** 1: BUSY 0: IDLE

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329C	AUXADC_STA1	AUXADC_STA1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_THR_MD	AUXADC_ADC_BUSY_IN_THR_HW	AUXADC_ADC_BUSY_IN_GPS	AUXADC_ADC_BUSY_IN_GPS_MD	AUXADC_ADC_BUSY_IN_GPS_AP	AUXADC_ADC_BUSY_IN_FGADC_SWCHR	AUXADC_ADC_BUSY_IN_FGADC_PCHR	AUXADC_ADC_BUSY_IN_IMP	AUXADC_ADC_BUSY_IN_SHARE	AUXADC_ADC_BUSY_IN_MDBG	AUXADC_ADC_BUSY_IN_MDRT	AUXADC_ADC_BUSY_IN_JEITA				
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_THR_MD	**ADC busy status** 1: BUSY 0: IDLE
14	AUXADC_ADC_BUSY_IN_THR_HW	**ADC busy status** 1: BUSY 0: IDLE
13	AUXADC_ADC_BUSY_IN_GPS	**ADC busy status** 1: BUSY 0: IDLE
12	AUXADC_ADC_BUSY_IN_GPS_MD	**ADC busy status** 1: BUSY 0: IDLE
11	AUXADC_ADC_BUSY_IN_GPS_AP	**ADC busy status** 1: BUSY 0: IDLE
10	AUXADC_ADC_BUSY_IN_FGADC_SWCHR	**ADC busy status** 1: BUSY 0: IDLE
9	AUXADC_ADC_BUSY_IN_FGADC_PCHR	**ADC busy status** 1: BUSY 0: IDLE
8	AUXADC_ADC_BUSY_IN_IMP	**ADC busy status** 1: BUSY 0: IDLE
7	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 1: BUSY 0: IDLE
6	AUXADC_ADC_BUSY_IN_MDBG	**ADC busy status** 1: BUSY 0: IDLE
5	AUXADC_ADC_BUSY_IN_MDRT	**ADC busy status** 1: BUSY 0: IDLE
4	AUXADC_ADC_BUSY_IN_JEITA	**ADC busy status** 1: BUSY 0: IDLE

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329E	AUXADC_STA2	AUXADC_STA2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_NAG												AUXADC_ADC_BUSY_IN_PWRON	AUXADC_ADC_BUSY_IN_BATID	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_SWCHR	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_PCHR
Type	RO												RO	RO	RO	RO
Reset	0												0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_NAG	**ADC busy status** 1: BUSY 0: IDLE
3	AUXADC_ADC_BUSY_IN_PWRON	**ADC busy status** 1: BUSY 0: IDLE
2	AUXADC_ADC_BUSY_IN_BATID	**ADC busy status** 1: BUSY 0: IDLE
1	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_SWCHR	**ADC busy status** 1: BUSY 0: IDLE
0	AUXADC_ADC_BUSY_IN_BAT_PLUGIN_PCHR	**ADC busy status** 1: BUSY 0: IDLE

3600	AUDDEC_ANA_CON0	AUDDEC Control Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRBSCCURRENT_VAUDP32	RG_AUDHPLBSCCURRENT_VAUDP32	RG_AUDHPRSCDISABLE_VAUDP32	RG_AUDHPLSCDISABLE_VAUDP32	RG_AUDHPRMUXINPUTSEL_VAUDP32		RG_AUDHPLMUXINPUTSEL_VAUDP32		RG_AUDHPRPWRUP_IBIAS_VAUDP32	RG_AUDHPLPWRUP_IBIAS_VAUDP32	RG_AUDHPRPWRUP_VAUDP32	RG_AUDHPLPWRUP_VAUDP32	RG_AUDDAC_PWL_UP_VA32	RG_AUDDAC_PWR_UP_VA32	RG_AUDDACRPWRUP_VAUDP32	RG_AUDDACLPWRUP_VAUDP32
Type	RW	RW	RW	RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDHPRBSCC	**Audio right headphone BSC current**

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Bit(s)	Name	Description
	URRENT_VAUDP32	
14	RG_AUDHPLBSCCURRENT_VAUDP32	**Audio left headphone BSC current**
13	RG_AUDHPRSCDISABLE_VAUDP32	**Disables headphone right short circuit protection**
12	RG_AUDHPLSCDISABLE_VAUDP32	**Disables headphone left short circuit protection**
11:10	RG_AUDHPRMUXINPUTSEL_VAUDP32	**Selects audio right headphone input multiplexor** Positive/negative pins: 00: Open/open 01: LOLP/LOLN 10: IDACRP/IDACRN 11: HSP/HSN (test mode)
9:8	RG_AUDHPLMUXINPUTSEL_VAUDP32	**Selects audio left headphone input multiplexo** Positive/negative pins: 00: Open/open 01: LOLP/LOLN 10: IDACRP/IDACRN 11: HSP/HSN (test mode)
7	RG_AUDHPRPWRUP_IBIAS_VAUDP32	**Audio right headphone bias power up**
6	RG_AUDHPLPWRUP_IBIAS_VAUDP32	**Audio left headphone bias power up**
5	RG_AUDHPRPWRUP_VAUDP32	**Audio right headphone power up**
4	RG_AUDHPLPWRUP_VAUDP32	**Audio left headphone power up**
3	RG_AUD_DAC_PWL_UP_VA32	**Power down control for left channel audio biasgen.** 0: Power down 1: Enable
2	RG_AUD_DAC_PWR_UP_VA32	**Power down control for right channel audio biasgen** 0: Power down 1: Enable
1	RG_AUDDACRPWRUP_VAUDP32	**Power down control for right-channel audio DAC.** 0: Power down 1: Enable
0	RG_AUDDACLPWRUP_VAUDP32	**Power down control for left-channel audio DAC.** 0: Power down 1: Enable

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3602	AUDDEC_ANA_CON1	AUDDEC Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_HPROUTSTGCTRL_VAUDP32			RG_HPLOUTSTGCTRL_VAUDP32			RG_HPRSHORT2HPRAUX_EN_VAUDP32	RG_HPLSHORT2HPLAUX_EN_VAUDP32	RG_HPRAUXFBRSW_EN_VAUDP32	RG_HPLAUXFBRSW_EN_VAUDP32	RG_AUDHPROUTAUXPWRUP_VAUDP32	RG_AUDHPLOUTAUXPWRUP_VAUDP32	RG_AUDHPROUTPWRUP_VAUDP32	RG_AUDHPLOUTPWRUP_VAUDP32
Type			RW			RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:11	RG_HPROUTSTGCTRL_VAUDP32	**Selects audio right headphone output stage** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x
10:8	RG_HPLOUTSTGCTRL_VAUDP32	**Selects audio left headphone output stage** 000: 1x 001: 2x 010: 3x 011: 4x 100: 5x 101: 6x 110: 7x 111: 8x
7	RG_HPRSHORT2HPRAUX_EN_VAUDP32	
6	RG_HPLSHORT2HPLAUX_EN_VAUDP32	**Enables audio left headphone main & aux output stages short**
5	RG_HPRAUXFBRSW_EN_VAUDP32	**Enables audio right headphone aux feedback resistor for audio depop**
4	RG_HPLAUXFBRSW_EN_VAUDP32	**Audio left headphone aux feedback resistor enable**
3	RG_AUDHPROUTAUXPWRUP_VAUDP32	**Audio right headphone aux output stage power up**
2	RG_AUDHPLOUTAUXPWRUP_VAUDP32	**Audio left headphone aux output stage power up**
1	RG_AUDHPROUTPWRUP_VAUDP32	**Audio right headphone main output stage power up**
0	RG_AUDHPLOUTPWRUP_VAUDP32	**Audio left headphone main output stage power up**

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3604 AUDDEC_ANA_CON2 AUDDEC Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_HPPSHORT2VCM_VAUDP32	RG_AUDREFN_DERES_EN_VAUDP32	RG_AUDHPSTARTUP_VAUDP32							RG_HPROUTPUTSTBENH_VAUDP32				RG_HPLOUTPUTSTBENH_VAUDP32		
Type	RW	RW	RW							RW				RW		
Reset	0	0	0							0	0	0		0	0	0

Bit(s)	Name	Description
15	RG_HPPSHORT2VCM_VAUDP32	**HP driver positive output stage short to AU_REFN**
14	RG_AUDREFN_DERES_EN_VAUDP32	**HP ESD resistor @AU_REFN short enable**
13	RG_AUDHPSTARTUP_VAUDP32	**Forces a Startup mode in HP Amps if required**
6:4	RG_HPROUTPUTSTBENH_VAUDP32	**Enhances HPR output stage STB** [2]: Reserved [1]: Enable HPRN SHORT2VCM [0]: HPR output stage STB enhance option 0: No enhancement 1: Enhance
2:0	RG_HPLOUTPUTSTBENH_VAUDP32	**Enhances HPL output stage STB** [2]: Reserved [1]: Enable HPLN SHORT2VCM [0]: HPL output stage STB enhance option 0: No enhancement 1: Enhance

3606 AUDDEC_ANA_CON3 AUDDEC Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_HPOUTPUTRESET0_VAUDP32	RG_HPINPUTRESET0_VAUDP32	RG_HPINPUTSTBENH_VAUDP32	RG_AUDHPTRIM_EN_VAUDP32	RG_AUDHPRFINETRIM_VAUDP32		RG_AUDHPLFINETRIM_VAUDP32		RG_AUDHPRTRIM_VAUDP32				RG_AUDHPLTRIM_VAUDP32			
Type	RW	RW	RW	RW	RW		RW		RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_HPOUTPUTRESET0_VAUDP32	**HPL/R driver SE output reset to 0V ground** 0: Not reset

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Bit(s)	Name	Description
		1: Reset
14	RG_HPINPUTRESETo_VAUDP32	**HP driver input reset to ground** 0: Not reset 1: Reset
13	RG_HPINPUTSTBENH_VAUDP32	**HP driver input stability enhance option** 0: No enhancement 1: Enhance
12	RG_AUDHPTRIM_EN_VAUDP32	**Enable control of trim circuit of HP** 0: Disable trim circuit 1: Enable trim circuit
11:10	RG_AUDHPRFINETRIM_VAUDP32	**Fine trim offset voltage of HPR** 01: -0.5mV 10: +0.5mV
9:8	RG_AUDHPLFINETRIM_VAUDP32	**Fine trim offset voltage of HPL** 01: -0.5mV 10: +0.5mV
7:4	RG_AUDHPRTRIM_VAUDP32	**Trims offset voltage of HPR** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
3:0	RG_AUDHPLTRIM_VAUDP32	**Trims offset voltage of HPL** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV

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3608	AUDDEC_ANA_CON4	AUDDEC Control Register 4	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPCOMP_EN_VAUDP32		RG_AUDHPHFCOMPBUFGAINSEL_VAUDP32			RG_AUDHPHFCOMPRESSEL_VAUDP32				RG_AUDHPLFCOMPRESSEL_VAUDP32				RG_AUDHPDIFFINPBIASADJ_VAUDP32		
Type	RW		RW			RW				RW				RW		
Reset	0		0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
15	RG_AUDHPCOMP_EN_VAUDP32	Reserved
13:12	RG_AUDHPHFCOMPBUFGAINSEL_VAUDP32	Reserved
10:8	RG_AUDHPHFCOMPRESSEL_VAUDP32	Reserved
6:4	RG_AUDHPLFCOMPRESSEL_VAUDP32	Reserved
2:0	RG_AUDHPDIFFINPBIASADJ_VAUDP32	Reserved

360A	AUDDEC_ANA_CON5	AUDDEC Control Register 5	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDHPDEDMGAINADJ_VAUDP32				RG_AUDHPDECMGAINADJ_VAUDP32		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	RG_AUDHPDEDMGAINADJ_VAUDP32	Reserved
2:0	RG_AUDHPDECMGAINADJ_VAUDP32	Reserved

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360C	AUDDEC_ANA_CON6	AUDDEC Control Register 6	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_HSOUT_SHORTVCM_VAUDP32	RG_HSOUTPUTRESET0_VAUDP32	RG_HSINPUTRESET0_VAUDP32	RG_HSINPUTSTBENH_VAUDP32	RG_HSOUTPUTSTBENH_VAUDP32	RG_AUDHSSTARTUP_VAUDP32	RG_AUDHSBSCCURRENT_VAUDP32	RG_AUDHSSCDISABLE_VAUDP32	RG_AUDHSMUXINPUTSEL_VAUDP32		RG_AUDHSPWRUP_IBIAS_VAUDP32	RG_AUDHSPWRUP_VAUDP32
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_HSOUT_SHORTVCM_VAUDP32	**Short HS output to VCM (DCC: 0V; ACC: 1.4V)** 0: Not short to VCM 1: Short to VCM
10	RG_HSOUTPUTRESET0_VAUDP32	**HS driver DE outputs reset to 0V ground** 0: No reset 1: Reset
9	RG_HSINPUTRESET0_VAUDP32	**HS driver DE inputs reset to 0V ground** 0: No reset 1: Reset
8	RG_HSINPUTSTBENH_VAUDP32	**HS driver input stability enhance option** 0: No enhancement 1: Enhance
7	RG_HSOUTPUTSTBENH_VAUDP32	**HS driver output stability enhance option** 0: No enhancement 1: Enhance
6	RG_AUDHSSTARTUP_VAUDP32	**Forces a Startup mode in HS Amp if required**
5	RG_AUDHSBSCCURRENT_VAUDP32	**Audio handset BSC current**
4	RG_AUDHSSCDISABLE_VAUDP32	**Disables headset short circuit protection**
3:2	RG_AUDHSMUXINPUTSEL_VAUDP32	**Selects audio handset input multiplexor** Positive/negative pins: 00: Open/open 01: MUTE (input grounded) 10: Voice playback 11: Test mode
1	RG_AUDHSPWRUP_IBIAS_VAUDP32	**Audio headset bias power up**
0	RG_AUDHSPWRUP_VAUDP32	**Audio headset power up**

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360E	AUDDEC_ANA_CON7	AUDDEC Control Register 7	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_LOOUT_SHORTVCM_VAUDP32	RG_LOOUTPUTRESET0_VAUDP32	RG_LOINPUTRESET0_VAUDP32	RG_LOOUTPUTSTBENH_VAUDP32	RG_LOINPUTSTBENH_VAUDP32	RG_AUDLOSTARTUP_VAUDP32	RG_AUDLOLBSCCURRENT_VAUDP32	RG_AUDLOLSCDISABLE_VAUDP32	RG_AUDLOLMUXINPUTSEL_VAUDP32		RG_AUDLOLPWRUP_IBIAS_VAUDP32	RG_AUDLOLPWRUP_VAUDP32
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_LOOUT_SHORTVCM_VAUDP32	**Short LO output to VCM (DCC: 0V; ACC: 1.4V)** 0: Not short to VCM 1: Short to VCM
10	RG_LOOUTPUTRESET0_VAUDP32	**LOL/R driver SE output reset to 0V ground** 0: No reset 1: Reset
9	RG_LOINPUTRESET0_VAUDP32	**LO driver input reset to ground** 0: No reset 1: Reset
8	RG_LOOUTPUTSTBENH_VAUDP32	**LO driver output stability enhance option** 0: No enhancement 1: Enhance
7	RG_LOINPUTSTBENH_VAUDP32	**LO driver input stability enhance option** 0: No enhancement 1: Enhance
6	RG_AUDLOSTARTUP_VAUDP32	**Forces a Startup mode in LO Amps if required**
5	RG_AUDLOLBSCCURRENT_VAUDP32	**Audio left LO buffer BSC current**
4	RG_AUDLOLSCDISABLE_VAUDP32	**Disables LO buffer left short circuit protection**
3:2	RG_AUDLOLMUXINPUTSEL_VAUDP32	**Selects audio left LO buffer input multiplexo** Positive/negative pins 00: Open/open 01: MUTE (input grounded) 10: Audio playback 11: Test mode
1	RG_AUDLOLPWRUP_IBIAS_VAUDP32	**Audio left LO buffer bias power up**
0	RG_AUDLOLPWRUP_VAUDP32	**Audio left LO buffer power up**

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3610 **AUDDEC_ANA_CON8** **AUDDEC Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_AUDHPSPKDET_EN_VAUDP32	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP32		RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP32			RG_AUDTRIMBUF_EN_VAUDP32	RG_AUDTRIMBUF_GAINSEL_VAUDP32		RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP32			
Type				RW	RW		RW			RW	RW		RW			
Reset				0	0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
12	RG_AUDHPSPKDET_EN_VAUDP32	**Enables audio headphone speaker detection**
11:10	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP32	**Selects audio headphone speaker detection output mux** 00: Open 01: HPL 10: HPR 11: Unused
9:8	RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP32	**Enables audio headphone speaker detection input mux** 00: Open 01: DACLP 10: DACLN 11: DACRP
6	RG_AUDTRIMBUF_EN_VAUDP32	**Enables audio offset trimming buffer**
5:4	RG_AUDTRIMBUF_GAINSEL_VAUDP32	**Selects audio offset trimming buffer gain** 00: 0dB 01: 6dB 10: 12dB 11: 18dB
3:0	RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP32	**Selects audio offset trimming buffer mux** 0000: Open 0001: HP+N65+N69

3612 **AUDDEC_ANA_CON9** **AUDDEC Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD0_VAUDP32								RG_ABIDEC_RSVD0_VA32							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD0_VAUDP32	**Reserved one byte in VAUDP32 domain** [7]: Enable HPRN/HPLN output 4K to VCM [6:4]: HP Aux loop gain setting [3]: Enable HPR aux CMFB loop [2]: Enable HPL aux CMFB loop [1]: Enable HPR/L main CMFB loop

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Bit(s)	Name	Description
		[0]: Enable HP output stage turn on timing control
7:0	RG_ABIDEC_RSVD0_VA32	**Reserved one byte in VA32 domain**

3614 AUDDEC_ANA_CON10 AUDDEC Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RSVD2_VAUDP32								RG_ABIDEC_RSVD1_VAUDP32							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RSVD2_VAUDP32	Reserved one byte in VAUDP32 domain
7:0	RG_ABIDEC_RSVD1_VAUDP32	Reserved one byte in VAUDP32 domain

3616 AUDDEC_ANA_CON11 AUDDEC Control Register 11 4900

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDBIASADJ_0_VAUDP32												RG_AUDZCDCLKSEL_VAUDP32	RG_AUDZCDMUXSEL_VAUDP32		
Type	RW												RW	RW		
Reset	0	1	0	0	1	0	0	1	0				0	0	0	0

Bit(s)	Name	Description
15:7	RG_AUDBIASADJ_0_VAUDP32	**Audio bias adjustment 0, bits:** [2:0] Headphone Left/Right DR bias current setting [5:3] Handset DR bias current setting. DR bias settings [8:6] Line-out DR bias current setting. DR bias settings 000: 4uA 001: 5uA 010: 6uA 011: 7uA 100: 8uA 101: 9A 110: 10uA 111: 11uA
3	RG_AUDZCDCLKSEL_VAUDP32	**Increases ZCD comparator speed** 0: Normal speed 1: Improved speed
2:0	RG_AUDZCDMUXSEL_VAUDP32	**Selects Zero Crossing Detection mux** 000: LOL 001: Unused

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Bit(s)	Name	Description
		010: Handset 011: Unused 100: Bypass ZCD

3618	AUDDEC_ANA_CON12	AUDDEC Control Register 12	0155

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_AUDIBIASPWRDN_VAUDP32	RG_AUDBIASADJ_1_VAUDP32							
Type								RW	RW							
Reset								1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
8	RG_AUDIBIASPWRDN_VAUDP32	**Power down control for IbiasDistrib circuit** 0: Enable 1: Disable
7:0	RG_AUDBIASADJ_1_VAUDP32	**Audio bias adjustment 1, bits:** [7:6] ZCD bias current setting 00: 3uA 01: 4uA 10: 5uA 11: 6uA [5:4] LOL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [3:2] HS ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [1:0]: HPL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA

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361A **AUDDEC_ANA_CON13** **AUDDEC Control Register 13** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDGLB_LP2_VOW_EN_VA32	RG_AUDGLB_LP_VOW_EN_VA32	RG_AUDGLB_PWRDN_VA32		RG_SEL_DELAY_VCORE	RG_SEL_DECODER_96K_VA32	RG_RSTB_DECODER_VA32
Type										RW	RW	RW		RW	RW	RW
Reset										0	0	1		0	0	0

Bit(s)	Name	Description
6	RG_AUDGLB_LP2_VOW_EN_VA32	**Enable for AUDGLB VOW low-power mode2: OP and self-bias will be down and IREF from PMU_TOP**
5	RG_AUDGLB_LP_VOW_EN_VA32	**Enable for AUDGLB VOW low-power mode: OP and self-bias should be on, IREF to VOW is 1/4.**
4	RG_AUDGLB_PWRDN_VA32	**Power down control for audio global bias circuit** 0: Enable 1: Disable; default on
2	RG_SEL_DELAY_VCORE	**Selects AFIFO read clock delay** 0: 5ns 1: 10ns
1	RG_SEL_DECODER_96K_VA32	**Selects audio DAC clock** 0: 6.5MHz 1: 13MHz
0	RG_RSTB_DECODER_VA32	**Audio decoder reset** 0: Reset 1: Normal

361C **AUDDEC_ANA_CON14** **AUDDEC Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDPMU_RSVD_VA18										RG_NVREG_PULLOW_VAUDP32	RG_NVREG_EN_VAUDP32		RG_LCLDO_DEC_REMOTE_SENSE_VA18	RG_LCLDO_DEC_PDDIS_EN_VA18	RG_LCLDO_DEC_EN_VA32
Type	RW										RW	RW		RW	RW	RW
Reset	0	0	0	0	0	0	0	0			0	0		0	0	0

Bit(s)	Name	Description
15:8	RG_AUDPMU_RSVD_VA18	**Reserved 1 byte for VA18 domain** [7:4]: NCP SW1~SW4 individual off control 4'b0000: On (normal operation) 4'b1111: All off

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Bit(s)	Name	Description
		[3]: Reserved [2]: NCP clock low-bouncing control 0: Low-bouncing 1: Normal mode [1:0]: CLDO power MOS control 2'b00: Normal operation 2'b11: CLDO Vout=AVDD18_AUD
5	RG_NVREG_PULL0V_VAUDP32	**Reserved**
4	RG_NVREG_EN_VAUDP32	**Enable for NVREG**
2	RG_LCLDO_DEC_REMOTE_SENSE_VA18	**Selects LCLDO_DEC remote sense function** 0: Local sense 1: Remote sense
1	RG_LCLDO_DEC_PDDIS_EN_VA18	**Enables LCLDO_DEC power down discharge**
0	RG_LCLDO_DEC_EN_VA32	**Enable for LCLDO_DEC**

361E **AUDENC_ANA_CON0** **AUDENC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCLINPUTSEL		RG_AUDADCLPWRUP	RG_BULKL_VCM_EN	RG_AUDPREAMPLGAIN			RG_AUDPREAMPLINPUTSEL		RG_AUDPREAMPLVSCALE		RG_AUDPREAMPLPGATEST	RG_AUDPREAMPLDCPRECHARGE	RG_AUDPREAMPLDCCEN	RG_AUDPREAMPLON
Type		RW		RW	RW	RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCLINPUTSEL	**Selects audio L ADC input** 00: Idle 01: AIN0 10: Left preamplifier 11: Idle
12	RG_AUDADCLPWRUP	**Powers up audio L ADC** 0: Power down 1: Power on
11	RG_BULKL_VCM_EN	**Audio L preamplifier PGA Switch bulk tied to VCM or supply rail control** 0: Tied to supply rail 1: Tied to VCM
10:8	RG_AUDPREAMPLGAIN	**Adjusts audio L preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB

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Bit(s)	Name	Description
7:6	RG_AUDPREAMPL INPUTSEL	**Selects audio L preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPL VSCALE	**Audio L preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPL PGATEST	**Enables audio L preamplifier PGA test** 0: Disable
2	RG_AUDPREAMPL DCPRECHARGE	**Audio L preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPL DCCEN	**Audio L DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPL ON	**Enables audio L preamplifier** 0: Disable 1: Enable

3620 **AUDENC_ANA_CON1** **AUDENC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDADCRINPUTSEL		RG_AUDADCRPWRUP	RG_BULKR_VCM_EN	RG_AUDPREAMPRGAIN			RG_AUDPREAMPRINPUTSEL		RG_AUDPREAMPRVSCALE		RG_AUDPREAMPRPGATEST	RG_AUDPREAMPRDCPRECHARGE	RG_AUDPREAMPRDCCEN	RG_AUDPREAMPRON
Type		RW		RW	RW	RW			RW		RW		RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:13	RG_AUDADCRINP UTSEL	**Selects audio R ADC input** 00: Idle 01: AIN0 10: Right preamplifie 11: Idle
12	RG_AUDADCRPWR UP	**Powers up audio R ADC** 0: Power down 1: Power on
11	RG_BULKR_VCM_ EN	**Audio R preamplifier PGA Switch bulk tied to VCM or supply rail control** 0: Tied to supply rail 1: Tied to VCM
10:8	RG_AUDPREAMPR GAIN	**Adjusts audio R preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB

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Bit(s)	Name	Description
7:6	RG_AUDPREAMPR INPUTSEL	**Selects audio R preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPR VSCALE	**Audio R preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPR PGATEST	**Enables audio R preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPR DCPRECHARGE	**Audio R preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPR DCCEN	**Audio R DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPR ON	**Enables audio R preamplifier** 0: Disable 1: Enable

3622 AUDENC_ANA_CON2 AUDENC Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCFLASHIDDTEST		RG_AUDADCREFBUFIDDTEST		RG_AUDADC2NDSTAGEIDDTEST		RG_AUDADC1STSTAGEIDDTEST		RG_AUDPREAMPIDDTEST		RG_AUDADCFLASHLPEN	RG_AUDADC2NDSTAGELPEN	RG_AUDADC1STSTAGELPEN	RG_AUDPREAMPLPEN	RG_AUDGLBVOWLPWEN	RG_AUDULHALFBIAS
Type	RW		RW		RW		RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_AUDADCFLASHIDDTEST	**Selects audio ADC flash Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
13:12	RG_AUDADCREFBUFIDDTEST	**Selects audio ADC reference buffer Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
11:10	RG_AUDADC2NDSTAGEIDDTEST	**Audio ADC 2nd & 3rd stage Idd adjust bits** 00: 100% 01: 80% 10: 120% 11: 140%
9:8	RG_AUDADC1STSTAGEIDDTEST	**Audio ADC 1st stage Idd adjust bits** 00: 100% 01: 80%

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Bit(s)	Name	Description
		10: 120% 11: 140%
7:6	RG_AUDPREAMPIDDTEST	**Audio preamplifier Idd adjust bits** 00: 100% 01: 75% 10: 125% 11: 150%
5	RG_AUDADCFLASHLPEN	**Enables audio ADC flash low power** 0: Normal 1: Enable
4	RG_AUDADC2NDSTAGELPEN	**Enables audio ADC 2nd & 3rd low power** 0: Normal 1: Enable
3	RG_AUDADC1STSTAGELPEN	**Enables audio ADC 1st stage low power** 0: Normal 1: Enable
2	RG_AUDPREAMPLPEN	**Audio preamplifier PGA low power mode** 0: Disable 1: Enable
1	RG_AUDGLBVOWLPWEN	**Enables audio uplink globe bias VOW low power mode** 0: Normal 1: Enable
0	RG_AUDULHALFBIAS	**Enables audio uplink halfbias** 0: Normal 1: Enable

3624 **AUDENC_ANA_CON3** **AUDENC Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREPGA					RG_DCCVCMBUFLPSWEN	RG_DCCVCMBUFLPMODSEL	RG_AUDPREAMPAAFEN	RG_AUDADCDAC0P25FS	RG_AUDADCCLKGENMODE		RG_AUDADCCLKSOURCE		RG_AUDADCCLKSEL		RG_AUDADCCLKRSTB
Type	RW					RW	RW	RW	RW	RW		RW		RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:11	RG_AUDSPAREPGA	**0: RG_NNP_EN_VA25** 1: SWenh1_VA25 2: SWenh2_VA25 3: OP_CMFBEN_VA25
10	RG_DCCVCMBUFLPSWEN	**Audio preamplifier PGA DCC VCM buffer SW EN**
9	RG_DCCVCMBUFLPMODSEL	**Audio preamplifier PGA DCC VCM buffer LP MODSEL**
8	RG_AUDPREAMPAAFEN	**Audio preamplifier PGA with AAF input in DC couple mode** 0: Disable 1: Enable

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Bit(s)	Name	Description
7	RG_AUDADCDAC0P25FS	**Enables audio ADC FBDAC 0.25FS** 0: 13MHz clock in, 6.5MHz data out 1: 3.25MHz clock in, 1.625MHz data out
6:5	RG_AUDADCCLKGENMODE	**Audio ADC clock gen. mode** 00: Divided by 2 (normal) 01: Divided by 4 10: Divided by 8 11: Not divided
4:3	RG_AUDADCCLKSOURCE	**Audio ADC clock source** 00: 13MHz from CLKSQ 01: VOW test from CLKSQ 10: 12.58MHz from 32kHz PLL 11: 12MHz ring oscillator
2:1	RG_AUDADCCLKSEL	**Selects audio ADC's filter adjustment for clock** 00: For 13MHz clock in, 6.5MHz data out 10: For 26MHz clock in, 13MHz data out 01: For 6.5MHz clock in, 3.25MHz data out 11: NA
0	RG_AUDADCCLKRSTB	**Audio ADC clock RSTB** 0: Reset 1: Enable

3626 **AUDENC_ANA_CON4** **AUDENC Control Register 4** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDADCDACTEST	RG_AUDADCNODEM	RG_AUDADCDACNRZ	RG_AUDADCDACIDDTEST		RG_AUDADCDACFBCURRENT	RG_AUDADCFFBYPASS	RG_AUDADCBYPASS	RG_AUDADCNOPATEST	RG_AUDADCWIDECM	RG_AUDADCFSRESET	RG_AUDADC3RDSTAGERESET	RG_AUDADC2NDSTAGERESET	RG_AUDADC1STSTAGESDENB
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	RG_AUDADCDACTEST	**Audio ADC DAC test** 0: Disable 1: Enables the data in RG_AUDADCTESTDATA[15:0] to be passed to the DAC
12	RG_AUDADCNODEM	**Audio ADC DEM test**
11	RG_AUDADCDACNRZ	**Audio ADC DAC in non return to zero mode** 0 RZ mode (2I) 1 NRZ mod (I)
10:9	RG_AUDADCDACIDDTEST	**Audio ADC-DAC Idd current test selection** 00: Normal 11 -20% DAC f/b current
8	RG_AUDADCDACFBCURRENT	**Audio ADC feedback coefficient**
7	RG_AUDADCFFBY	**Audio ADC feed forward bypass**

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Bit(s)	Name	Description
	PASS	0 no bypass, allow feedforward coefficient to pass signal to ADC flash 1 bypass, don't allow ADC i/p signal to feedforward flash
6	RG_AUDADCBYPASS	**Audio ADC input resistor bypass enable** 0: Disable 1: Enable
5	RG_AUDADCNOPATEST	**Audio ADC no preamp test** 0: Normal ADC gain 1: 6dB ADC gain
4	RG_AUDADCWIDECM	**Enables audio ADC wide common mode** 0: Normal 1: Enable
3	RG_AUDADCFSRESET	**Selects audio encoder FS reset block model**
2	RG_AUDADC3RDSTAGERESET	**Audio ADC 3rd stage reset** 0: Normal 1: Reset
1	RG_AUDADC2NDSTAGERESET	**Audio ADC 2nd stage reset** 0: Normal 1: Reset
0	RG_AUDADC1STSTAGESDENB	**Audio ADC 1st stage source degenerate enableb** 0: Enable 1: Disable

3628 AUDENC_ANA_CON5 AUDENC Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCTESTDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_AUDADCTESTDATA	**Audio ADC test data bits** Audio ADC test data bits for both phases of DRTZ DAC. Can enable any current source you choose.

362A AUDENC_ANA_CON6 AUDENC Control Register 6 1515

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDRCTUNERSEL	RG_AUDRCTUNER							RG_AUDRCTUNELSEL	RG_AUDRCTUNEL				
Type			RW	RW							RW	RW				
Reset			0	1	0	1	0	1			0	1	0	1	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
13	RG_AUDRCTUNER SEL	**Audio R ADC RC tuning select** 0 Use auto cal tune bits 1 use RG_AUDRCTUNEL[4:0]
12:8	RG_AUDRCTUNER	**Audio R ADC RC tuned value** See RG_AUDRCTUNELSE
5	RG_AUDRCTUNEL SEL	**Audio L ADC RC tuning select** 0 Use auto cal tune bits 1 use RG_AUDRCTUNEL[4:0]
4:0	RG_AUDRCTUNEL	**Audio L ADC RC tuned value** See RG_AUDRCTUNELSE

362C **AUDENC_ANA_CON7** **AUDENC Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_AUDRCTUNERREAD								RGS_AUDRCTUNELREAD				
Type				RO								RO				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
12:8	RGS_AUDRCTUNERREAD	Audio R RC tune read data
4:0	RGS_AUDRCTUNELREAD	Audio L RC tune read data

362E **AUDENC_ANA_CON8** **AUDENC Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVA18								RG_AUDSPAREVA30							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_AUDSPAREVA18	Spare control bits for AVDD18 voltage domain
7:0	RG_AUDSPAREVA30	Spare control bits for AVDD30 voltage domain

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3630	AUDENC_ANA_CON9	AUDENC Control Register 9	0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVMIC				RG_DMICMONSEL			RG_DMICMONEN	RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_DMICHPCLKEN	RG_AUDDIGMICBIAS		RG_AUDDIGMICEN
Type	RW				RW			RW	RW		RW		RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_AUDSPAREVMIC	**Spare control bits for AVDD25MIC voltage domain**
11:9	RG_DMICMONSEL	**Enable digital microphone monitor path enable**
8	RG_DMICMONEN	**Enable digital microphone monitor path** 0: Disable 1: Enable
7:6	RG_AUDDIGMICNDUTY	**Digital microphone negative duty control**
5:4	RG_AUDDIGMICPDUTY	**Digital microphone positive duty control**
3	RG_DMICHPCLKEN	**Selects enable digital microphone monitor path** 0: Digital CLK 1: CLKSQ
2:1	RG_AUDDIGMICBIAS	**Digital microphone slew rate control** 11 > 10 > 01 > 00
0	RG_AUDDIGMICEN	**Enables digital microphone** 0: Disable 1: Enable

3632	AUDENC_ANA_CON10	AUDENC Control Register 10	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDMICBIAS0DCSW2NEN	RG_AUDMICBIAS0DCSW2P2EN	RG_AUDMICBIAS0DCSW2P1EN	RG_AUDPWDBMICBIAS2	RG_AUDMICBIAS0LOWPEN	RG_AUDMICBIAS0VREF			RG_AUDMICBIAS0DCSW0NEN	RG_AUDMICBIAS0DCSW0P2EN	RG_AUDMICBIAS0DCSW0P1EN	RG_AUDPWDBMICBIAS0
Type					RW	RW	RW	RW	RW	RW			RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_AUDMICBIAS0DCSW2NEN	**MIC Bias 2 DC couple switch 0N** 0: Off 1: On
10	RG_AUDMICBIAS0DCSW2P2EN	**MIC Bias 2 DC couple switch 0P2** 0: Off 1: On

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Bit(s)	Name	Description
9	RG_AUDMICBIAS0DCSW2P1EN	**MIC Bias 2 DC couple switch 0P1** 0: Off 1: On
8	RG_AUDPWDBMICBIAS2	**MIC Bias 2 power down** 0: Power down 1: Power on
7	RG_AUDMICBIAS0LOWPEN	**Enables MIC Bias 0 Low Power** 0: Normal mode 1: Low power mode
6:4	RG_AUDMICBIAS0VREF	**Selects MIC Bias 0 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: 2.6V 111: 2.7V
3	RG_AUDMICBIAS0DCSW0NEN	**MIC Bias 0 DC couple switch 0N** 0: Off 1: On
2	RG_AUDMICBIAS0DCSW0P2EN	**MIC Bias 0 DC couple switch 0P2** 0: Off 1: On
1	RG_AUDMICBIAS0DCSW0P1EN	**MIC Bias 0 DC couple switch 0P1** 0: Off 1: On
0	RG_AUDPWDBMICBIAS0	**MIC Bias 0 power down** 0: Power down 1: Power on

3634 **AUDENC_ANA_CON11** **AUDENC Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_BANDGAPGEN	RG_AUDMICBIAS1HVVREF	RG_AUDMICBIAS1HVEN	RG_AUDMICBIAS1LOWPEN	RG_AUDMICBIAS1VREF				RG_AUDMICBIAS1DCSW1NEN	RG_AUDMICBIAS1DCSW1PEN	RG_AUDPWDBMICBIAS1
Type						RW	RW	RW	RW	RW				RW	RW	RW
Reset						0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
10	RG_BANDGAPGEN	**Remote sense to bandgap ground** 0: Disable 1: Enable
9	RG_AUDMICBIAS1HVVREF	**Selects high voltage output voltage** 0: 2.85V 1: 2.8V

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Bit(s)	Name	Description
8	RG_AUDMICBIAS1HVEN	**High voltage enable for mic detection** 0: Disable 1: Enable
7	RG_AUDMICBIAS1LOWPEN	**Enables MIC Bias 1 Low Power** 0: Normal mode 1: Low power mode
6:4	RG_AUDMICBIAS1VREF	**Selects MIC Bias 1 output voltage** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.5V 110: 2.6V 111: 2.7V
2	RG_AUDMICBIAS1DCSW1NEN	**MIC Bias 1 DC couple switch 1N** 0: Off 1: On
1	RG_AUDMICBIAS1DCSW1PEN	**MIC Bias 1 DC couple switch 1P** 0: Off 1: On
0	RG_AUDPWDBMICBIAS1	**MIC Bias 1 power down** 0: Power down 1: Power on

3636 **AUDENC_ANA_CON12** **AUDENC Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ACCDETSPAREVA30			RG_EINTCONFIGACCDET	RG_EINTCOMPVTH	RG_SWBUFSWEN	RG_SWBUFMODSEL	RG_ACCDETSEL	RG_AUDACCDETTVDET	RG_AUDACCDETVTHBCAL	RG_AUDACCDETVTHACAL	RG_EINTHIRENB	RG_AUDACCDETVIN1PULLLOW	RG_AUDACCDETMICBIAS2PULLLOW	RG_AUDACCDETMICBIAS1PULLLOW	RG_AUDACCDETMICBIAS0PULLLOW
Type	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:13	RG_ACCDETSPAREVA30	**Spare control bits for ACCDET**
12	RG_EINTCONFIGACCDET	**Enables EINT pull high resistor**
11	RG_EINTCOMPVTH	**EINT comparator threshold** 0: 2.8V 1: 2.4V
10	RG_SWBUFSWEN	**Switch buffer turn on SW mode control for ACCDET to AUXADC** 0: Power down 1: Power on

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Bit(s)	Name	Description
9	RG_SWBUFMODSEL	**Buffer power control** 0: Hardware mode 1: Software mode
8	RG_ACCDETSEL	**Selects ACCDET input** 0: ACCDET pin 1: MICP pin
7	RG_AUDACCDETTVDET	**Put audio accessory detection into TV mode** 0: Disable 1: Enable
6	RG_AUDACCDETVTHBCAL	**Audio accessory detection voltage threshold B calibration**
5	RG_AUDACCDETVTHACAL	**Audio accessory detection voltage threshold A calibration**
4	RG_EINTHIRENB	**Selects EINT High R** 0: 2M 1: 500k
3	RG_AUDACCDETVIN1PULLLOW	**Pull low VIN1 pads when MICBIAS is off** 0: Disable 1: Enable
2	RG_AUDACCDETMICBIAS2PULLLOW	**Pull low MIC Bias 2 pads when MICBIAS is off** 0: Disable 1: Enable
1	RG_AUDACCDETMICBIAS1PULLLOW	**Pull low MIC Bias 1 pads when MICBIAS is off** 0: Disable 1: Enable
0	RG_AUDACCDETMICBIAS0PULLLOW	**Pull low MIC Bias 0 pads when MICBIAS is off** 0: Disable 1: Enable

3638 AUDENC_ANA_CON13 AUDENC Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDENCSPAREVA18								RG_AUDENCSPAREVA30							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_AUDENCSPAREVA18	Spare control bits for AVDD18 voltage domain
7:0	RG_AUDENCSPAREVA30	Spare control bits for AVDD30 voltage domain

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363A	AUDENC_ANA_CON14	AUDENC Control Register 14	0310

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLL_PDIV1				RG_PLL_PDIV1_EN	RG_PLL_RLATCH_EN	RG_PLL_DIV1						RG_PLL_DCKO_SEL		RG_PLLBS_RST	RG_PLL_EN
Type	RW				RW	RW	RW						RW		RW	RW
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:12	RG_PLL_PDIV1	**Div. no of post div. (Divider for FGADC)** Ratio = (N+2)*2
11	RG_PLL_PDIV1_EN	**post-div1: Enable. (Divider for FGADC)**
10	RG_PLL_RLATCH_EN	**Enables fbdiv relatch** 0: Disable 1: Enable
9:4	RG_PLL_DIV1	**Div. no of fbk divider** Ratio = (N+2)*16
3:2	RG_PLL_DCKO_SEL	**Reserved**
1	RG_PLLBS_RST	**Enables PLL reset** 1'b0: Disable 1'b1: Enable
0	RG_PLL_EN	**Enables PLL CLK** 0: Disable 1: Enable

363C	AUDENC_ANA_CON15	AUDENC Control Register 15	0180

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLL_DCHP_EN	RG_PLL_HPM_EN	RG_PLL_CKT_EN	RG_PLL_VCT_EN	RG_PLL_CKT_SEL		RG_PLL_IBSEL		RG_CKO_SEL		RG_PLL_BR		RG_PLL_BP		RG_PLL_BC	
Type	RW	RW	RW	RW	RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_PLL_DCHP_EN	**Reserved**
14	RG_PLL_HPM_EN	**Reserved**
13	RG_PLL_CKT_EN	**Enables clock test mode** 0: Disable 1: Enable
12	RG_PLL_VCT_EN	**Enables v-control test mode** 0: Disable

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Bit(s)	Name	Description
		1: Enable
11:10	RG_PLL_CKT_SEL	**Selects ck test mode** 00: CKI_RTC 01: 32k from PLL 10: 406kHz 11: CK_VCO
9:8	RG_PLL_IBSEL	**Selects PLL bias current** 00: 0.5u 01: 1.0u 10: 1.5u 11: 2.0u
7:6	RG_CKO_SEL	**Selects cko to FGADC** 00: RTC 01: 32k from PLL 10: 406kHz 11: XX
5:4	RG_PLL_BR	**Adjusts P-path resistance** 00: 800kohm 01: 400kohm 10: 150kohm 11: 150kohm
3:2	RG_PLL_BP	**Adjusts P-path capacitance** 00: 6pF 01: 8pF 10: 10pF 11: 12pF
1:0	RG_PLL_BC	**Adjusts I-path capacitance** 00: 15pF 01: 20pF 10: 25pF 11: 30pF

363E **AUDENC_ANA_CON16** **AUDENC Control Register 16** **0013**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_PLL_RSVA								RG_PLL_DCHP_AEN	RG_CKDRV_EN	RG_VCOBAND			RG_PLL_CDIV		
Type	RW								RW	RW	RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

Bit(s)	Name	Description
15:8	RG_PLL_RSVA	**Reserved**
7	RG_PLL_DCHP_AEN	**Reserved**
6	RG_CKDRV_EN	**Enables clock test mode** 0: Disable 1: Enable
5:3	RG_VCOBAND	**Selects manual PLL band** 000: R-band = 16k

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Bit(s)	Name	Description
		001: R-band = 4k 010: R-band = 8k 100: R-band = 12k
2:0	RG_PLL_CDIV	**Time domain cap multiplication ratio** 000: X1 001: X2 011: X4 111: X8

3800 **<u>ZCD_CON0</u>** **ZCD Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_AUDZCDMUXSEL_VAUDP15**				**RG_AUDZCDTIMEOUTMODESEL**	**RG_AUDZCDGAINSTEPSIZE**		**RG_AUDZCDGAINSTEPTIME**			**RG_AUDZCDENABLE**
Type						RW				RW	RW		RW			RW
Reset						0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
10:8	RG_AUDZCDMUXSEL_VAUDP15	**Selects zero crossing detection mux** 000: LineL and LineR 001: HPL and HPR 010: Handset 011: IV buffer 100: Bypass ZCD 000: Left line in & Right line in 001: Headphone L & headphone R 010: Handset 011: IV buffer 100: bypass ZCD 101: Bypass ZCD 110: Bypass ZCD 111: Bypass ZCD
6	RG_AUDZCDTIMEOUTMODESEL	**If no zero crossings are detected over a period of 30ms/5ms, a timeout will occur and ZCD block enter SILENT mode** 0: 30ms 1: 5ms
5:4	RG_AUDZCDGAINSTEPSIZE	**Gain step size to change the internal gain of ZCD** 00: 1dB. 01: 2dB. 10: 4dB. 11: 8dB.
3:1	RG_AUDZCDGAINSTEPTIME	**Gain step time to change the internal gain of ZCD** 000: 0 us. 001: 250 us 010: 500 us. 011: 1 ms. 100: 2 ms. 101: 4 ms. 110: 8 ms. 111: 16 ms.

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Bit(s)	Name	Description
0	RG_AUDZCDENABLE	**Enable for zero crossing detection (ZCD) function** 0: Disable 1: Enable

3802 ZCD_CON1 ZCD Control Register 1 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDLORGAIN							RG_AUDLOLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDLORGAIN	00000: +8dB 00001: +7dB 10010:-10dB 11111: -40dB (mute) 00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).
4:0	RG_AUDLOLGAIN	00000: +8dB 00001: +7dB 10010:-10d 11111: -40dB (mute) 00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).

3804 ZCD_CON2 ZCD Control Register 2 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPRGAIN							RG_AUDHPLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDHPRGAIN	00000: +8dB 00001: +7dB 10010:-10dB 11111: -40dB (mute) 00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).
4:0	RG_AUDHPLGAIN	00000: +8dB 00001: +7dB 10010:-10dB 11111: -40dB (mute) 00000: +8dB. 00001: +7dB. 10010: -10dB

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Bit(s)	Name	Description
		11111: -40dB(Mute).

3806 ZCD_CON3 ZCD Control Register 3 001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_AUDHSGAIN				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	RG_AUDHSGAIN	00000: +8dB 00001: +7dB 10010:-10dB 11111: -40dB (mute) 00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).

3808 ZCD_CON4 ZCD Control Register 4 0707

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDIVRGAIN								RG_AUDIVLGAIN		
Type						RW								RW		
Reset						1	1	1						1	1	1

Bit(s)	Name	Description
10:8	RG_AUDIVRGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB 000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB
2:0	RG_AUDIVLGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB 000: +5dB

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Bit(s)	Name	Description
		001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB

380A **ZCD_CON5** **ZCD Control Register 5** **3F3F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDINTGAIN2								RG_AUDINTGAIN1					
Type			RO								RO					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
13:8	RG_AUDINTGAIN2	Monitor signal: internal gain2
5:0	RG_AUDINTGAIN1	Monitor signal: internal gain1

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4 Application Notes

4.1 Hardware External Shutdown

The following schematic illustrates the hardware external shut-down function for MT6355 to power down when the main chip software crashes.

- Short press PWRKEY or HOMEKEY
  - INT-> EINT -> software control
  - Power-down, sleep mode or the other functions
- Long press shut-down
  - Force power-off of PMU
  - 5/8/11/14 s with < 20% accuracy
  - External reset function with source from:
    - PWRKEY and HOMEKEY both pressed for a long period of time
    - PWRKEY pressed for a long period of time
    - HOMEKEY pressed for a long period of time
  - Software disables watchdog counter.

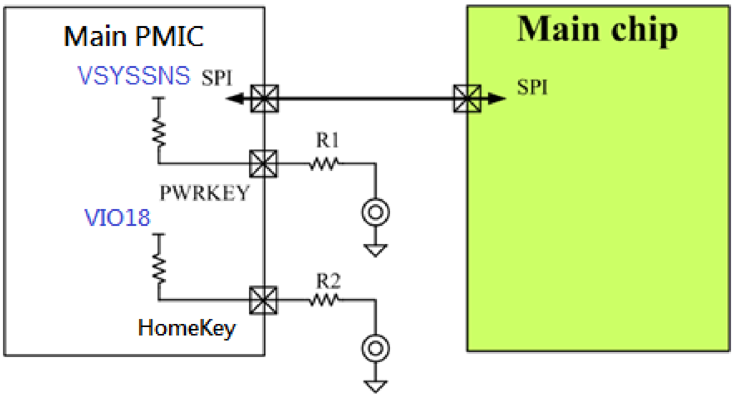

Figure 4-1. Hardware external shut-down function

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4.2 Configuration for Unused Buck Converter

The figure below shows the configuration for MT6355 buck converters that is not used.

- Configuration for VPA not in use:
  – Connect VBAT_PA to VBAT; connect GND_PA to GND
  – VPA & VPA_FB: Floating
  – RG_VPA_EN = 0 & RG_VPA_NDIS_EN = 1 (software setting)

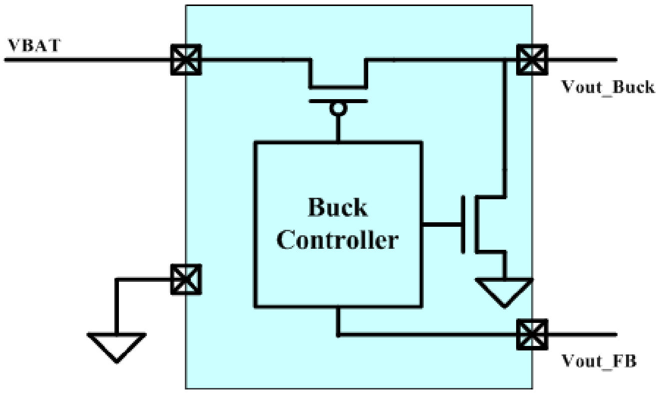

Figure 4-2. Configuration for unused DC/DC

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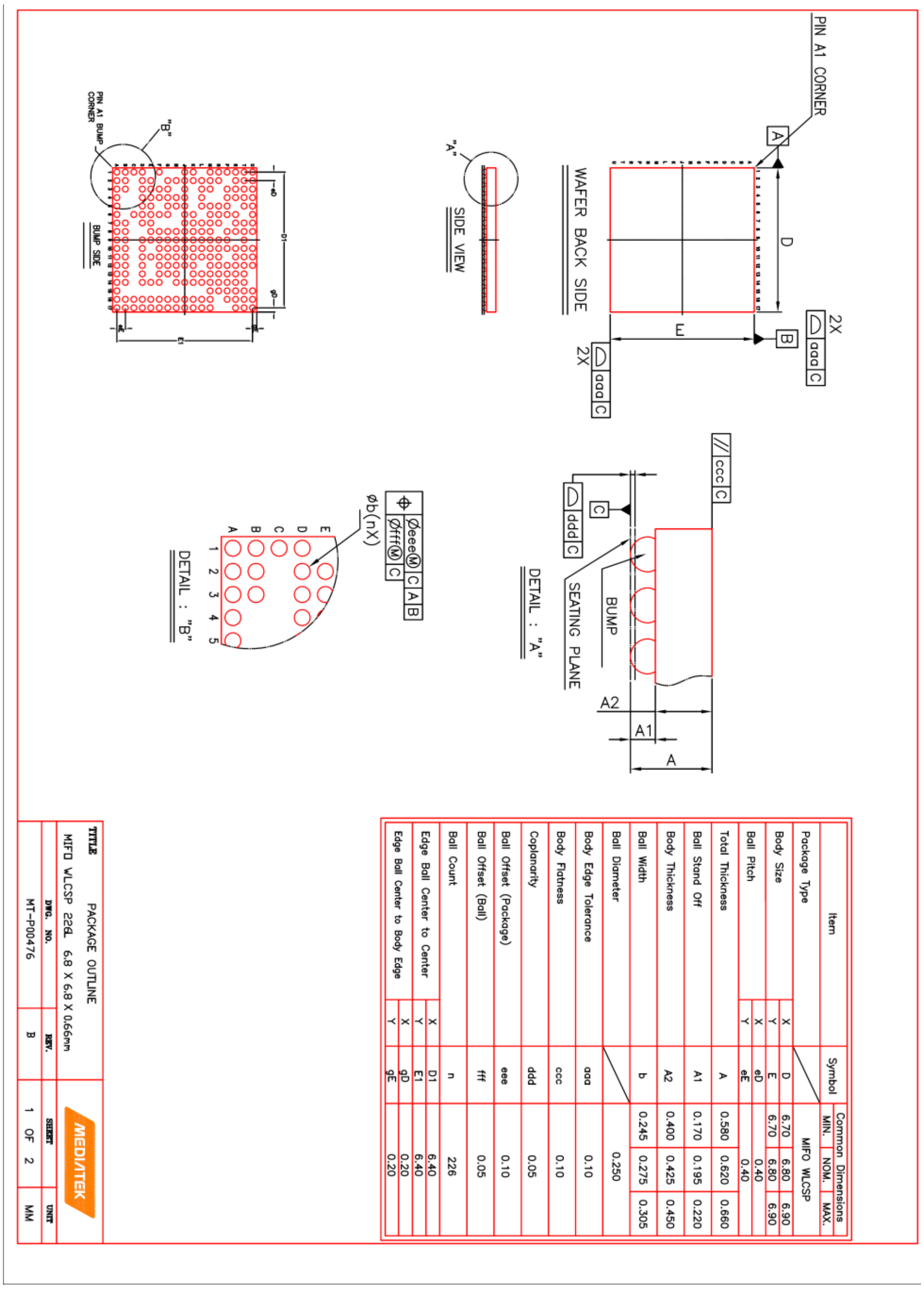
5 MT6355 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				MIFO WLCSP	
Body Size	X	D	6.70	6.80	6.90
	Y	E	6.70	6.80	6.90
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Total Thickness		A	0.580	0.620	0.660
Ball Stand Off		A1	0.170	0.195	0.220
Body Thickness		A2	0.400	0.425	0.450
Ball Width		b	0.245	0.275	0.305
Ball Diameter				0.250	
Body Edge Tolerance		aaa		0.10	
Body Flatness		ccc		0.10	
Coplanarity		ddd		0.05	
Ball Offset (Package)		eee		0.10	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		226	
Edge Ball Center to Center	X	D1		6.40	
	Y	E1		6.40	
Edge Ball Center to Body Edge	X	gD		0.20	
	Y	gE		0.20	

Figure 5-1. Package dimension

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Appendix

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